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Paper 59
Entered: July 6, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

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IPR2025-00191
Patent 11,581,322 B2

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Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL T. CYGAN, *Administrative Patent Judges*.

CYGAN, *Administrative Patent Judge*.

# DECISION
## Final Written Decision
## Determining Some Challenged Claims Unpatentable
## *35 U.S.C. § 318(a)*

# I. INTRODUCTION

## *A. Background and Summary*

Micron Technology, Inc. ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–20 of U.S. Patent No. 11,581,322 B2 (Ex. 1001, "the '322 patent"). Paper 1 ("Pet."). The Petition is supported by a Declaration from Dr. Jack C. Lee. Ex. 1003 ("Lee Declaration"). Yangtze Memory Technologies Company, Ltd. ("Patent Owner") filed a Preliminary Response to the Petition. Paper 12 ("Prelim. Resp."). The Preliminary Response is supported by a Declaration by Dr. Stephen Campbell. Ex. 2007. On February 21, 2025, Patent Owner filed a Statutory Disclaimer of claims 1, 2, 4, 5, and 7; thus, we treat claims 1, 2, 4, 5, and 7 as having never been part of the '322 patent. Ex. 2006; *see Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1383 (Fed. Cir. 1998) ("This court has interpreted the term 'considered as part of the original patent' in [35 U.S.C.] § 253 to mean that the patent is treated as though the disclaimed claims never existed."). The non-disclaimed claims that remain challenged by the present Petition are claims 3, 6, and 8–20. Paper 22 ("Inst. Dec.")

Patent Owner filed a Brief on Discretionary Denial, and Petitioner filed a brief in opposition. Papers 10 and 18. The Director considered the briefing and determined that discretionary denial was not warranted. Paper 21. On July 25, 2025, we instituted an *inter partes* review of claims 3, 6, and 8–20, which are all of the remaining non-disclaimed claims of the '322 patent challenged in this proceeding.

On November 17, 2025, Patent Owner filed a Response. Paper 34 ("Resp."). The Response is supported by a second Declaration by Dr. Stephen Campbell. Ex. 2021 ("Campbell Resp. Dec."). On February 9, 2026, Petitioner filed a Reply Brief. Paper 47 ("Pet. Reply"). Petitioner's

Reply Brief is supported by a second Declaration by Dr. Jack C. Lee, and is accompanied by a transcript of a deposition of Dr. Campbell. Exs. 1105 ("Lee Reply Dec."), 1106 ("Campbell Dep."). On March 3, 2026, Patent Owner filed a Sur-reply, accompanied by a transcript of a deposition of Dr. Lee. Paper 55 ("Sur-reply"); Ex. 2038. We held an Oral Hearing with the parties on July 30, 2025, and a transcript was entered into the record. Paper 58 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons explained below, Petitioner establishes by a preponderance of the evidence that claims 3, 8, 11, 12, and 19 are unpatentable, and that Petitioner does not establish by a preponderance of evidence that challenged claims 6, 9, 10, 13–18, and 20 are unpatentable.

### *B. Real Parties-in-Interest*

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as real parties-in-interest. Pet. 6. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1.

### *C. Related Matters*

The parties represent that the '322 patent is involved in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023). Paper 5, 1; Pet. 6–7. Petitioner also filed twenty three IPRs challenging each patent asserted in the district court case. Pet. 7–8.

### *D. The '322 Patent*

The '322 patent is titled "Three-Dimensional Memory Devices Having Through Array Contacts and Methods for Forming the Same."

Ex. 1001, code (54). The '322 patent issued on February 14, 2023, from application No. 17/100,847, filed on November 21, 2020, and is a division of application No. 16/745,342, now U.S. Patent 11,049,866, which is a division of U.S. Application Number 16/149,103, filed on October 1, 2018, which is now U.S. Patent 10,566,336, which in turn is a continuation of Application Number PCT/CN2018/101482, filed on August 21, 2018. *Id.* at codes (21), (22), (63).

The '322 patent relates to a staircase structure for a 3D memory device including a dielectric stack, including a plurality of dielectric/conductor layer pairs, having a channel structure extending vertically therethrough. *Id.* at code (57). A dummy channel structure filled with a dielectric layer is formed vertically in an opening in the dielectric stack. *Id.* Figure 1 of the '322 patent illustrates the structure:

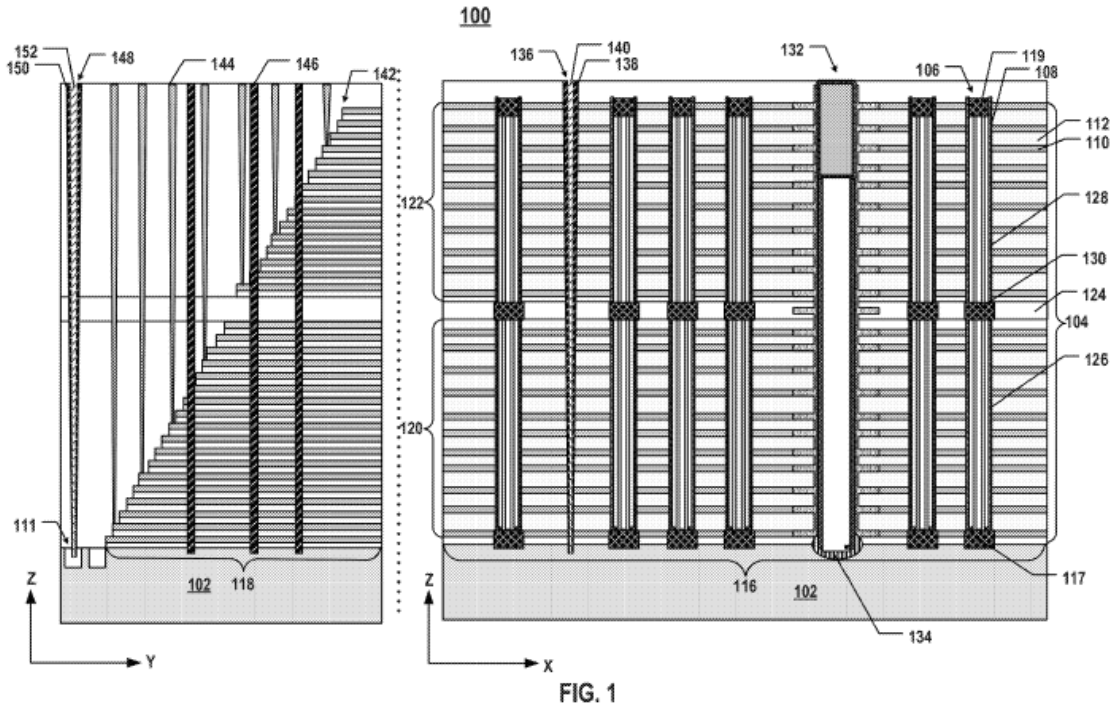

FIG. 1

Ex. 1001, Fig. 1. Figure 1 depicts memory device 100 having memory stack 104 including interleaved conductor layers 110 and dielectric layers 112,

which includes channel structure 108 filled with semiconductor, and dummy channel structure 146 that is either filled with the same materials as those in channel structure 108 but lacking a connective contact, or is filled with dielectric materials. *Id.* at 5:23–7:4, 9:29–9:40.

### *E. Illustrative Claim*

Claims 1 (disclaimed), 8, and 14 are independent. Claim 14 is illustrative because it contains each of the limitations disputed by Patent Owner, and recites as follows:[1]

[14.PRE] A three-dimensional (3D) memory device, comprising:

[14.A] a substrate;

[14.B] a memory stack on the substrate and comprising a plurality of conductor/dielectric layer pairs;

[14.C] a channel structure extending vertically through the conductor/dielectric layer pairs in the memory stack;

[14.D] a through array contact (TAC) extending vertically through the conductor/dielectric layer pairs in the memory stack and buried into the substrate, the TAC comprising a substantially circular section; and

[14.E] a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack,

[14.F] wherein: a first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs; and

[1] Bracketed organization added as per the Petition. Pet. xvii–xviii.

[14.G] a peripheral contact is arranged outside the memory stack and in contact with a peripheral device on the substrate.

*F. Evidence*

Petitioner relies on the following patent document evidence.

| Name | Patent Document | Exhibit |
|---|---|---|
| Nishikawa et al. , "Nishikawa" | US 9,837,431 B2 | 1005 |
| Lu et al., ("Lu") | US 9,853,046 B2 | 1006 |
| Nishikawa et al., ("Nishikawa123")[2] | US 9,935,123 B2 | 1046 |

*G. Asserted Grounds*

Petitioner asserts that claims 3, 6, 8–15, 17, 18, and 20 would have been unpatentable on the following grounds:[3]

| Claim(s) Challenged | 35 U.S.C. § | Reference(s)/Basis |
|---|---|---|
| 3, 6, 8–10, 13–16, 19–20 | 103[4] | Nishikawa |
| 11, 12, 17, 18 | 103 | Nishikawa, Lu |
| 3, 6, 8–10, 13–16, 19–20 | 103 | Nishikawa, Nishikawa123 |
| 11, 12, 17, 18 | 103 | Nishikawa, Nishikawa123, Lu |

Pet. 10.

[2] Petitioner refers to this reference as "Nishikawa2."

[3] Although Petitioner challenged claims 1–20, this proceeding does not include disclaimed claims 1, 2, 4, 5, and 7.

[4] We apply AIA 35 U.S.C. § 103 to the '322 patent because it was filed after, and never claimed the benefit of an effective filing date before, March 16, 2013. Ex. 1001, codes (22), (63); Pet. 6.

## II. DISCUSSION

### *A. Legal Standards*

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103; *see also KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.[5] *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

### *B. Level of Ordinary Skill in the Art*

Petitioner asserts that a person of ordinary skill in the art ("POSITA") at the critical time "would have had a Bachelor of Science degree in electrical engineering or a similar discipline, along with 2–3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience)." Pet. 27 (citing Ex. 1003 ¶¶34–38). Petitioner further asserts that a POSITA "would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts." *Id.* Patent Owner does

[5] Neither party presents evidence or arguments regarding objective evidence of non-obviousness. Pet. 100; PO. Resp.

not object to this assessment, except to the extent that "designing" includes circuit design. PO Resp. 9–10 (citing Ex. 2021 ¶ 35). Neither Patent Owner nor Dr. Campbell considers the obviousness of the claims to turn on the precise definition of the level or ordinary skill in the art. PO Resp. 10; Ex. 2021 ¶ 35. For purposes of this Decision, we adopt Petitioner's proposed level of ordinary skill, as it appears to be consistent with the specification of the '322 patent and the prior art of record.

### *C. Claim Construction*

Neither party proposes any express claim construction. Pet. 27 (stating claims should receive their "plain and ordinary meaning"); PO Resp. 10 (stating that Petitioner's challenges fail "under any reasonable construction"). In an *inter partes* review, we construe a patent claim "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). Under this standard, the words of a claim generally are given their "ordinary and customary meaning," which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). We determine no terms require express construction for purposes of this Decision.

### *D. Nishikawa*

Nishikawa is titled, "3D Semicircular Vertical NAND String With Recessed Inactive Semiconductor Channel Sections." Ex. 1005, code (54). Nishikawa describes a vertical memory device having dielectric separator structures protruding into a facing pair of sidewalls of a memory stack structure within a memory opening. *Id.* at code (57). Figure 1 is illustrative:

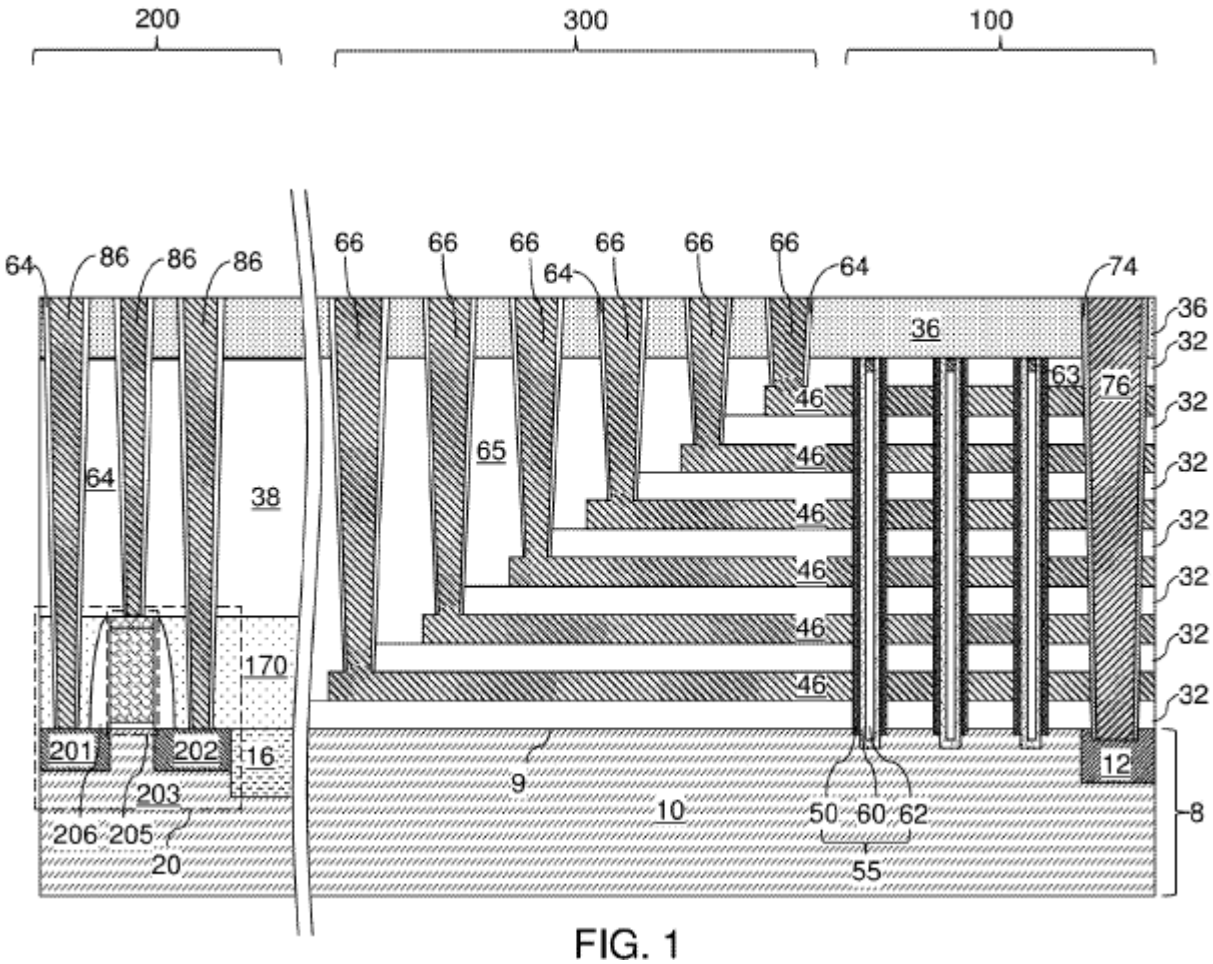


FIG. 1

Figure 1 depicts a 3D NAND stacked memory device having memory stack structures 55 (including memory film 50, semiconductor channel 60, and optionally a dielectric core 62) extending through an alternating stack of insulating layers 32 and conductive (optionally, sacrificial) layers 46, and backside contact via structure 76 providing electrical contact to source region 12. Ex. 1005, 4:22–6:57. Prior to the formation of backside contact via structure 76, etchant is introduced through a contact via stack at the backside contact regions to remove sacrificial material layers 42, which will be replaced with electrically conductive layers 46. *Id.* at 6:29–39.

*E. Nishikawa123*

Nishikawa123 is titled, "Within Array Replacement Openings for a Three-Dimensional Memory Device." Ex. 1046, code (54). Nishikawa123 describes reduction of backside trenches by using a subset of openings, which are otherwise employed as memory stack structures, to introduce etchant in a process of removing sacrificial material layers in an alternating stack of sacrificial and dielectric layers. *Id.* at code (57). Figure 16 is illustrative:

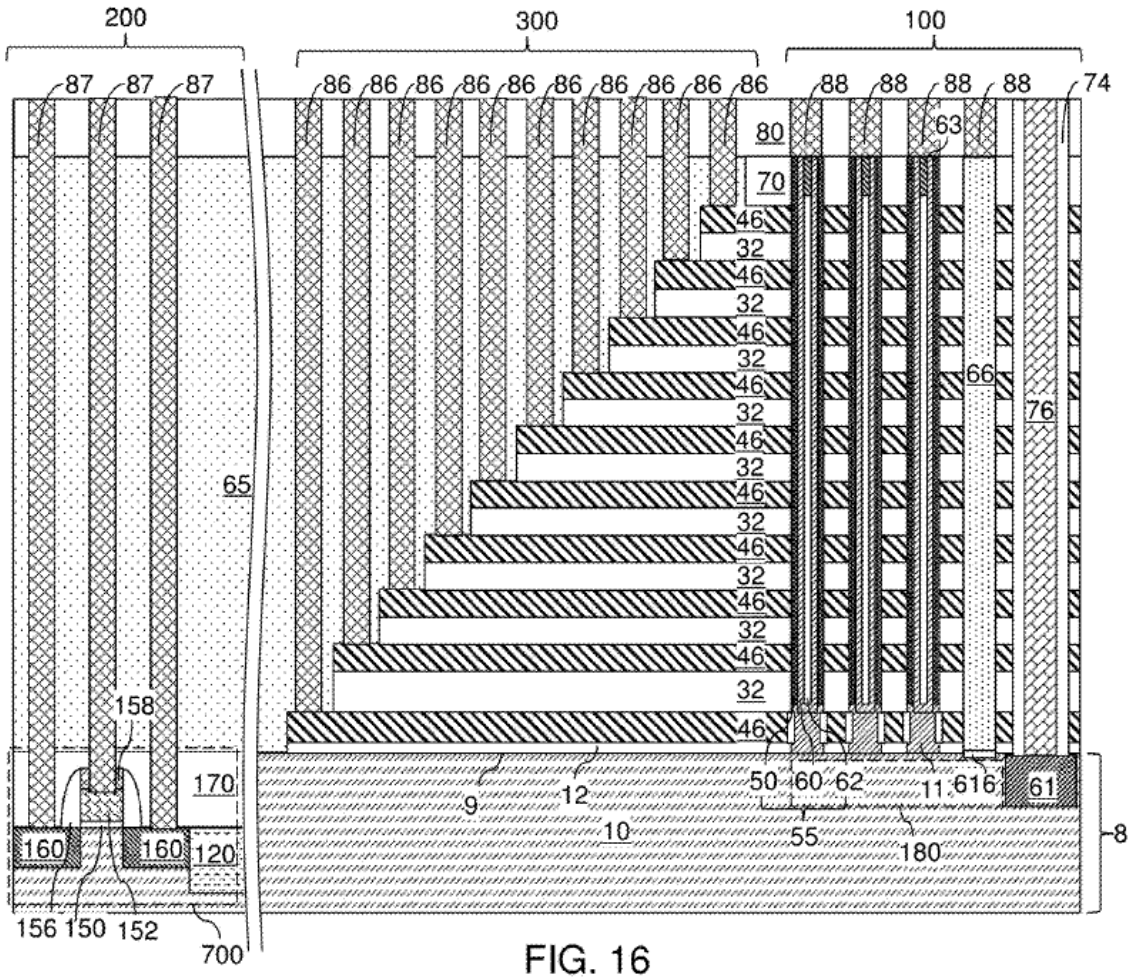


FIG. 16

Figure 16 depicts a 3D memory device including an alternating stack of insulating (23) and conductive (46) layers, memory stack structures 55,

dielectric pillar 66, and backside contact via structure 76. Ex. 1046, 25:55–26:17. Figure 17 provides a top-down view:

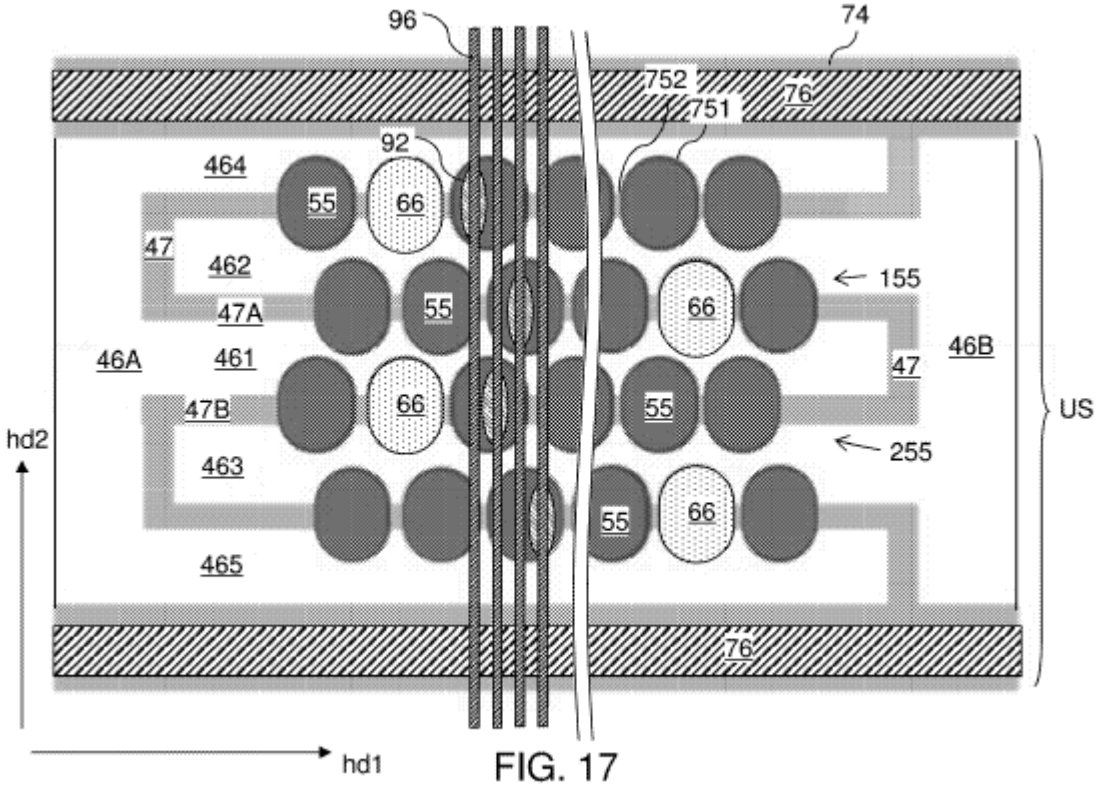


FIG. 17

Figure 17 depicts backside contact via structures 76, dielectric pillars 76, memory stack structures 55, and insulator structures 47, 47A, 47B which separate two sets of interdigitated conductive portions 46A, 46B. *Id.* at 26:7–54.

### *F. Claims 3, 6, 8–10, 13–16, and 19–20 over Nishikawa alone or in combination with Nishikawa123*

Petitioner asserts Nishikawa alone or in combination with Nishikawa123 renders obvious claims 3, 6, 8–10, 13–16, and 19–20.

Patent Owner asserts Petitioner has not shown that the asserted art teaches all of the limitations of the challenged claims. In particular, Patent Owner contests Petitioner's assertions for a TAC having a substantially circular section, a limitation present in claims 8–20. PO Resp. 10–30.

Patent Owner also contests Petition's assertions relating to a dummy channel structure as present in claims 3, 6, 14–18, and 20. Additionally, Patent Owner contests Petitioner's assertions regarding the different lateral dimensions of conductor/dielectric pairs as present in claims 13–18 and 20.

Because claim 14 includes each of these limitations, we begin our discussions with claim 14. Further, because Petitioner relies on Nishikawa123 either explicitly (Ground 2) or as representative of the knowledge in the art (Grounds 1), and Patent Owner addresses Petitioner's Grounds 1 and 2 arguments together, we follow that structure in our analysis.

*1. "substantially circular section" (claims 8–20)*

With respect to the TAC comprising "a substantially circular section" as recited in limitation 14.D, Petitioner asserts that it would have been obvious to replace Nishikawa's trench-shaped backside contact via structure with a circular-shaped backside via structure. Pet. 43. Petitioner asserts that Nishkawa123 states that its backside trench may have a circular shape, and that Nishikawa123's TACs provide the same structure as Nishikawa's TACs. *Id.* (citing Ex. 1005, Figs. 1, 16; Ex. 1046, Figs. 16, 17; Ex. 1003 ¶115). Petitioner points to other prior art demonstrating the well-known nature of circular TACs, including their use in a gate replacement process. *Id.* at 44–50. Petitioner asserts that such prior art teachings demonstrate that replacing a backside contact with a circular TAC was a known technique that would have been a suitable option for Nishikawa's trench and trench contact. *Id.* at 43–51. Petitioner further provides advantages of a circular TAC to replace the trench in Nishikawa: (1) the smaller footprint frees space for other components, and (2) multiple individual TACs may be spread through the array to provide closer contact points. *Id.* at 51–52.

*a) Patent Owner's Inoperability/Undesirability Arguments (Grounds 1 and 2)*

Patent Owner argues that modifying Nishikawa's trench-shaped TAC to a circular shape would "nullify Nishikawa's stated purpose and render Nishikawa inoperable." PO Resp. 11 (citing Ex. 2021 ¶ 49). Patent Owner annotates Nishikawa's Figure 16 as a depiction of its TAC ("backside contact via structure" 76):

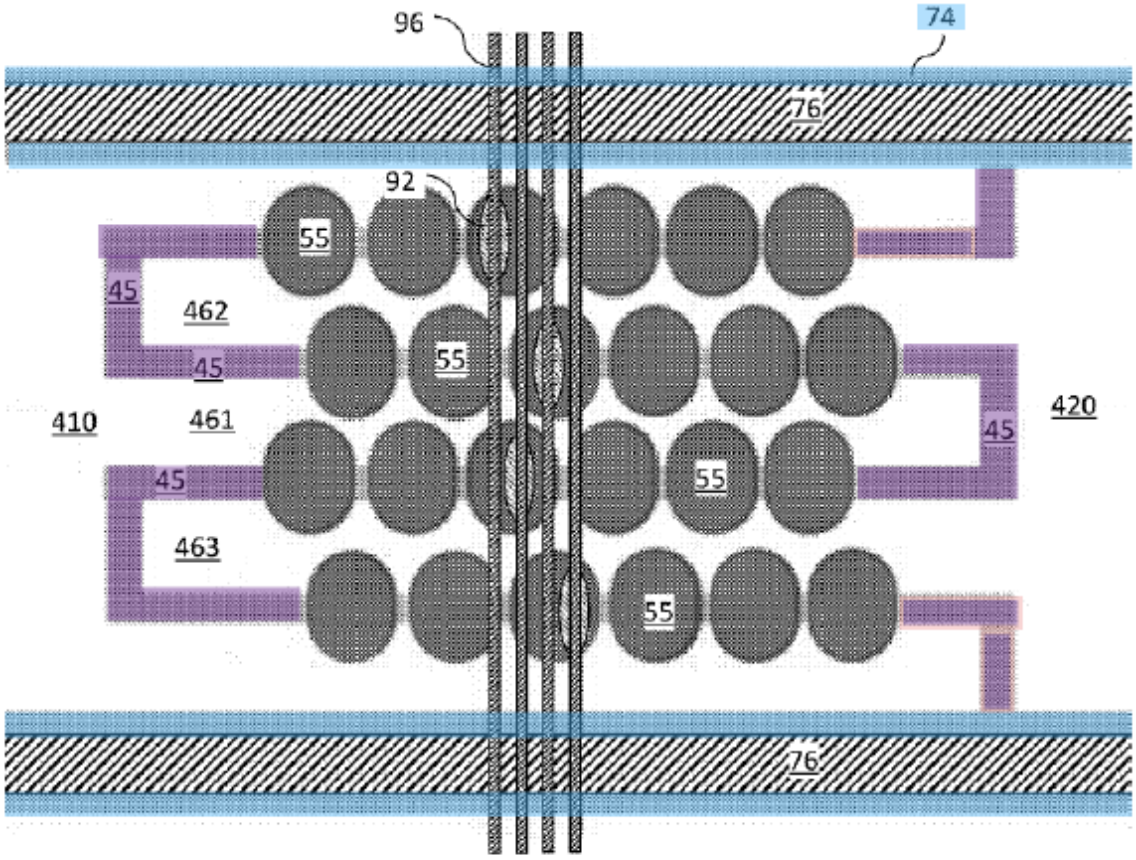


FIG. 16

Annotated Figure 16 shows TAC 76 surrounded by dielectric spacer 74 (blue) that, in concert with separator dielectric structures 45 (purple), separates wordlines 410 (white, left side) and 420 (white, right side). *Id.* at 14; Ex. 1005, Fig. 16, 6:57–59, 17:14–23. Such isolation is averred to prevent incorrect reads and writes by adjacent memory cells. *Id.* at 16–17

(citing Ex. 2021 ¶ 55). Patent Owner presents potential modifications of Nishikawa and argues that no modification would result in an operable and desirable device.

Patent Owner proposes for consideration a modification in which the trench is reshaped to a circle at the terminal ends of the dielectric structures 45, shown in a modified version of Figure 16:

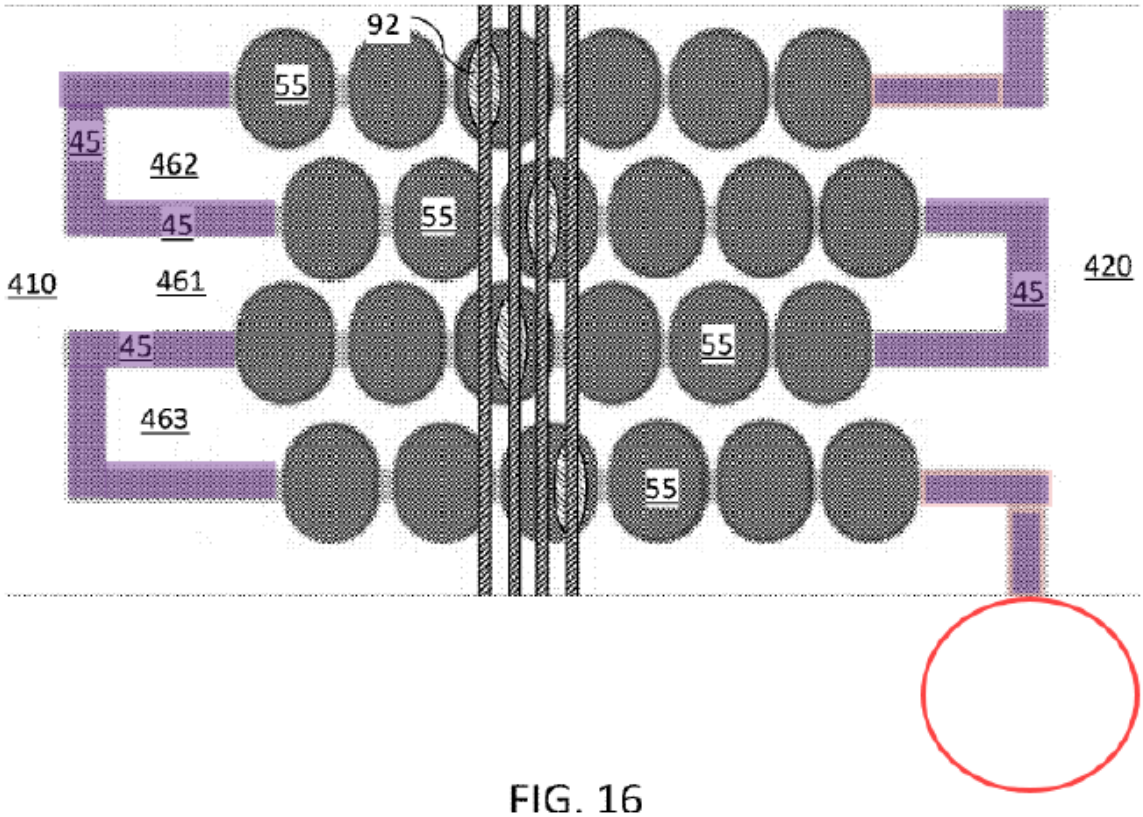


FIG. 16

**Nishikawa Fig. 16 (modified)**

Modified Figure 16 depicts a circular TAC "physically connected at the end of the separator dielectric structure 45" so as to "contact the side of the device to maintain the isolation." PO Resp. 22. Patent Owner argues that such a configuration is not suitable, citing Dr. Campbell's testimony that this circular TAC would require a larger footprint than a rectangular trench, and

Dr. Lee's testimony that a larger footprint is undesirable. *Id.* at 22 (citing Ex. 2021 ¶¶ 60–61).

We determine that such a configuration would be neither inoperable nor significantly undesirable. Dr. Campbell testified that he does not argue that this configuration would be inoperable. Ex. 1106, 74:12–17; Ex. 2021 ¶60. Dr. Lee testifies that this configuration is "consistent with Nishikawa[123]'s Figure 14B." Ex. 1105 ¶ 13. Dr. Lee further testifies that this configuration would not necessarily require a larger footprint, but instead, "could simply replace the trenches, abutting the device edge." *Id.* Dr. Campbell testified that if the circular TAC replaced the rectangular trench, "I don't know what it would be or exactly where it would be," and therefore, "I can't say what the size of the red circle would have to be." Ex. 1106, 83:19–84:3. Therefore, the record does not support finding a circular TAC to have a larger footprint. Absent a larger footprint, there is no evidence that the end-connected TAC would be undesirable.

Patent Owner argues that other proposed configurations would have drawbacks or be inoperable; however, because we have determined that at least one configuration is shown to be consistent with Nishikawa123's circular TAC embodiment and has not been shown to be undesirable, we need not consider other potential configurations. *See* PO Resp. 17–24. For example, Patent Owner also proposes that the structure resulting from Petitioner's modification of Nishikawa's trench would be a circular TAC located at the center of the trench. PO Resp. 17–22. However, although such a proposed modification is not disputed as being inoperable, both declarants testify that a person having ordinary skill in the art would not consider such a modification, and as Dr. Campbell attests, "Petitioner did

not propose such a modification." PO Resp. 17–22; Ex. 2021 ¶¶ 56–60; Ex. 1105 ¶¶ 8–10; Pet. Reply 2–3.

*b) Patent Owner's Ground 1 Arguments*

Patent Owner argues Petitioner improperly relies on "general knowledge" to supply the limitation of a TAC having a "substantially circular section" that is missing from Nishikawa. PO Resp. 29.

*(1) Arguments under 35 U.S.C. 311(b)*

First, Patent Owner argues that reliance on general knowledge, as exemplified by Nishikawa123 and other documents, is an improper basis for a proposed ground of rejection in an IPR petition. PO Resp. 29 (citing *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1373-75 (Fed. Cir. 2022) (stating that the "basis of a ground" must be "contained in a document that is a prior art patent or prior art printed publication") ("*Qualcomm I*").

Petitioner responds that because Nishikawa is prior art, the requirement of *Qualcomm* is satisfied. Pet. Reply 11.

The Federal Circuit revisited its *Qualcomm I* decision in *Qualcomm II*. *Qualcomm Incorporated v. Apple Inc.*, 134 F.4th 1355 (Fed. Cir. 2025) ("*Qualcomm II*"). In *Qualcomm II*, grounds that explicitly relied on evidence beyond prior art patents and publications were held to violate 35 U.S.C. § 311(b). *Qualcomm II*, 134 F.4th at 1366–67. In *Qualcomm II*, the Petition "prominently labeled" the basis of a ground to rely, at least in part, on "applicant's admitted art"; i.e., evidence that is neither a prior art patent nor publication. *Id.* at 1366. Moreover, the Petitioner in that case provided "express statements" that it formed the basis of that ground. *Id.* at 1367. Discussing *Qualcomm II*, the Federal Circuit stated that although "only patents and printed publications may form the basis of an IPR petition's unpatentability grounds. . . . general knowledge can be used to

supply a missing claim limitation." *Shockwave Med., Inc. v. Cardiovascular Sys., Inc.*, 142 F.4th 1371, 1378 (Fed. Cir. 2025).

In the Petition, Ground 1 is stated thusly: "**Ground 1:** Claims 1-3, 6, 7-10, 13-16, and 19-20 are obvious over Nishikawa." Pet. 10. Ground 1 is not explicitly based on a non-prior art reference or upon the general knowledge in the art or any other non-prior art evidence. There is some evidence to the contrary; for example, the Petition labels section heading X as "Ground 1: Nishikawa in view of the knowledge of a POSITA renders obvious Claims 1–3, 6–10, 13–16, and 19–20." However, each of the grounds has a section heading that states "in view of the knowledge of a POSITA," regardless of whether or not such knowledge is relied upon for a limitation missing in Nishikawa and not allegedly found in another prior art patent or publication named in that ground. *See, e.g.,* section heading XI ("Ground 2: Nishikawa in view of Nishikawa[123] and the knowledge of a POSITA"). Although close, we do not determine that the Petition "prominently labels" general knowledge as part of Ground 1 in a manner that would indicate reliance on general knowledge for an otherwise unaccounted element of the claim.

We further consider whether the Petition contains "express statements" that general knowledge forms the basis of the ground. The Petition contains numerous statements to the effect that replacing a backside contact or rectangular trench with a cylindrical or circular TAC was known in the art. *See* Pet. 43–51. The Petition also argues that such a modification would, even absent such knowledge, be obvious as providing a smaller footprint that would increase memory capacity, or by spreading common source connections throughout the array to provide closer contact points. *Id.* at 51–52. In the latter, Petitioner relies on Nishikawa's memory hole

openings as teaching the circular chape, using those openings as an alternative to its trench for the optional gate replacement process. In view of the inclusion of Nishikawa-only teaching of the circular TAC shape in its Nishikawa-based ground, we do not find clear express statements that Nishikawa lacks a circular teaching that may be combined with its trench teaching to supply the circular TAC limitation. Thus, under *Shockwave*, ground 1 does not violate 35 U.S.C. 311(b).

*(2) Arguments under 37 C.F.R. § 42.104(b)(4)*

Patent Owner also points to a memorandum from the USPTO on the use of general knowledge in a ground. PO Resp. 29–30 (citing USPTO Memorandum, Enforcement and Non-Waiver of 37 C.F.R. § 42.104(b)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews at 1 (July 31, 2025) ("General Knowledge Memorandum," https://www.uspto.gov/sites/default/files/documents/aapa_memo_final__signed.pdf)). Patent Owner argues that although this memo does not apply to the instant petition, it is evidence as to the USPTO's desired interpretation of 37 C.F.R. § 42.104(b)(4).

The General Knowledge Memorandum "imposes on petitioners a procedural requirement to identify in the petition where each claim element is found in the prior art patents or printed publications relied upon. General Knowledge Memorandum, 3. That Memorandum states that "as applied in some cases, [37 C.F.R. § 42.104(b)(4)] may be narrower than 35 U.S.C. §311(b)." *Id.* However, we determine that by setting an applicability date of "any petition for IPR filed on or after September 1, 2025" for the General Knowledge Memorandum, the Office intended to extend its "waiv[er of] enforcement of Rule 104(b)(4)" set by prior USPTO Memoranda for petitions filed prior to September 1, 2025. *Id.* at 1 n.1, 3. We are bound by

this intent and the prior USPTO Memoranda. Consequently, we decline to abbreviate the waiver set forth in the General Knowledge Memorandum, and do not rely on its provisions in this decision.

*(3) Appropriateness of general knowledge to supply a missing limitation*

Further relating to Ground 1, Patent Owner disputes Petitioner's reliance on general knowledge to "supplement the missing circular TAC limitation." PO Resp. 29.[6] Patent Owner argues that general knowledge cannot be so used unless "the record establishes the missing limitation is "***unusually simple***" and the "technology particularly ***straightforward***." *Id.* at 30 (citing *DSS Tech. Mgmt. v. Apple*, 885 F.3d 1367, 1374 (Fed. Cir. 2018)). Patent Owner argues that the pertinent technology applicable to all limitations is 3D NAND, which, like other highly technical electronic inventions, is "complex" and not "particularly straightforward." *Id.* at 31–35.

We disagree with Patent Owner's premise. In *DSS Tech*, the Federal Circuit held that reliance on "'ordinary creativity' 'as a wholesale substitute for reasoned analysis and evidence support'" without providing "a reasoned explanation that avoids conclusory generalizations" is not sufficient "when dealing with a limitation missing from the prior art references." 885 F.3d at 1376. There, the Federal Circuit explained that the Board did not identify any evidence to support its reliance on the ordinary creativity of the skilled artisan to supply the missing limitation. *See id.* at 1375; *see also id.* at 1376

[6] Although Patent Owner at one point states that this causes "all four grounds [to] fail on that basis alone" (PO Resp. 32), Grounds 2 and 4 rely on Nishikawa123, not background knowledge, for the circular TAC limitation (Pet. 98).

(stating that to the extent the Board relies on declarant testimony, such "conclusory statements and unspecific expert testimony" are insufficient to support the Board's findings). Consistent with concerns of hindsight bias and *ex post* reasoning, cases such as *DSS Tech* "reject[]obviousness determinations based on conclusory and unsupported expert testimony." *TQ Delta, LLC v. CISCO Sys., Inc.*, 942 F.3d 1352, 1361 (Fed. Cir. 2019).

Unlike the situation presented in *DSS Tech*, the Petition provides evidence to support its contention implementing Nishikawa's backside contact via cylindrical TACs was a suitable, well known option. *See e.g.,* Ex. 1003 ¶¶ 113–128 (citing, *inter alia*, Ex. 1005; Ex. 1010; Exs. 1020–1023; Ex. 1046). Patent Owner argues that Petitioner is "required to make [other references] part of the applicable obviousness combination." PO Resp. 31–32 n.5. However, Patent Owner presents no authority for such a requirement, which would conflict with the Federal Circuit's statement that "our case law has long recognized numerous permissible uses for general background knowledge in an IPR such as, 'for example, furnishing a motivation to combine, or supplying a missing claim limitation.'" *Shockwave*, 142 F.4th at 1378–79 (quoting *Qualcomm I*, 24 F.4th at 1376). *Shockwave* explicitly permits the use of evidence in an IPR to support an assertion that a missing claim limitation would have been obvious in view of general background knowledge. *Id.* at 1380; *see also K/S Himpp v. Hear-Wear Techs., LLC*, 751 F.3d 1362, 1365 (Fed. Cir. 2014) ("the Board was correct to require record evidence to support an assertion that the [claimed] features . . . were known prior art elements.").

The Petition does not merely provide a bare assertion that a circular shape would be suitable such it that relied upon common sense that would be unsuitable when contemplating a complex limitation involving a highly

technical issue, as was at issue in *DSS Tech. DSS Tech.*, 885 F.3d at 1374. Instead, the Petition provides multiple authorities to support its contention that circular TAC shapes were a known alternative to trench shapes in a manner consistent with Federal Circuit case law. *See, e.g., Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363–65 (Fed. Cir. 2016) (considering Petitioner's evidence where a missing limitation was not "evidently and indisputably within the common knowledge of those skilled in the art"). Consequently, we do not agree that Petitioner is barred from relying on evidence, outside of the prior art patents and publications listed in its grounds, to provide support for its contention that a limitation would have been obvious in view of the general knowledge in the art. [7]

*(4) Determination on Ground 1 Arguments*

For the above-described reasons, we do not agree with Patent Owner's Ground 1-specific arguments.

*c) Patent Owner's Ground 3 Arguments*

*(1) Standpoint of One of Ordinary Skill in the Art*

With respect to Ground 3, where Petitioner relies on Nishikawa123 for teaching the circular TAC, Patent Owner argues that obviousness is determined from the standpoint of one of ordinary skill in the art, not from the perspective of the inventors of a particular reference. PO Resp. 27–28. Patent Owner argues that Petitioner improperly asserts that a POSITA "would have considered potential improvements in Nishikawa[123] [over Nishikawa] given that its provisional was filed 5 days later" and by the same inventor. *Id.* (citing Pet. 99).

[7] As discussed, we reach this determination because the General Knowledge Memorandum does not apply to the instant Petition.

We do not agree with Patent Owner. Petitioner considered the combination from the standpoint of a person of ordinary skill in the art, not from the perspective of the inventors of the reference patents. Such consideration is entirely proper. *See KSR*, 550 U.S. at 402 ("a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle").

*(2) Patent Owner's Lack of Motivation to Modify Arguments*

Patent Owner argues that a POSITA would not have been motivated to modify Nishikawa to use Nishikawa123's circular TAC. PO Resp. 24. Patent Owner argues that to the extent that Figure 17 of Nishikawa123 is similar to Nishikawa's Figure 16, Nishikawa's 17 would not be understood to have a circular TAC. *Id.* Patent Owner distinguishes Nishikawa's discussion of Figure 17 from that of Figure 14, for which the alternatives of "circular, rectangular, or elongated trench shape" are described for opening 79. PO Sur-reply 11 (citing Ex. 1046, 22:39–41). Patent Owner states, "Nisihkawa123's teaching that the shape of an opening can be a "suitable shape, such as circular" does not apply to Nishikawa123's Figure 17," which like Figure 16 of Nishikawa, is an embodiment with a trench-shaped opening, not a circular one. PO Resp. 24–27 (citing Ex. 2021 ¶¶ 66–67; Ex. 1046, 25:32–35, Fig. 17). Patent Owner argues that the existence of a trench is optional in Nishikawa123, but its shape is tied to the particular embodiment. PO Sur-reply 12–13.

However, we agree with Petitioner that Nishikawa123 does not draw such a distinction. Pet. Reply 8. Nishikawa123 depicts comb-shaped electrodes and rectangular trenches in both Figure 14 and Figure 17. Ex. 1046, Fig. 14B, 17. Nishikawa123 describes each Figures 14 through 17 as "the exemplary [device] structure." Ex. 1046, 3:45–67. Dr. Lee testified

that Figures 14–17 described the same embodiment. Ex. 1105 ¶ 14. Dr. Campbell admitted that Figure 17 could represent the same embodiment as Figure 14. Ex. 1106, 100:22–101:3 (stating, "this wasn't described to be the same embodiment" while agreeing that "[i]t also wasn't described not to be the same embodiment," and concluding, "it certainly could be, but I don't know it."). Based on the above evidence, we agree with Petitioner that Nishikawa123 teaches its alternate shapes, including circular shapes, to apply to the embodiment or embodiments in Figures 14 through 17.

Consequently, we agree with Petitioner that Nishikawa123's teaching of a circular TAC as an alternative to an elongated trench would be applicable to the teachings of Nishikawa.

*d) Determination*

Consequently, we determine that Petitioner has sufficiently shown its contentions for Grounds 1 and 3 that Nishikawa alone, or in combination with Nishikawa123, teaches or suggests the "substantially circular section" recited in claim 14. We further determine that Petitioner has shown sufficient reason to modify Nishikawa's elongated trench to a circular shape; i.e., that the evidence of record supports Petitioner's assertion that replacing a backside contact with a circular TAC was a known technique that would be a suitable option for Nishikawa's trench and trench contact. Pet. 43–51; Ex. 1046, 22:38–41; Ex. 1009, 3:64–67; Ex. 1020, Fig. 8B, ¶ 96; Ex. 1003 ¶¶ 116–120; Ex. 1021, Fig. 1, 4:59–62; Ex. 1010, 110, 155; *see Randall Mfg. v. Rea*, 733 F.3d 1355, 1363 (Fed. Cir. 2013) ("Once it is established that a [feature was] prevalent, perhaps even predominant, . . . it is hard to see why one of skill in the art would not have thought to modify [the primary reference] to include this feature—doing so would allow the designer to

achieve the other advantages of the [primary reference] while using a [feature] that was very familiar in the industry.").

For the same reasons, Petitioner has also sufficiently shown a teaching of the "substantially circular section" recited in claims 8 and 19, and incorporated through dependency in claims 9–13, 15–18, and 20.

*2. "dummy channel structure" (claims 3, 6, 14–18, 20)*

Claims 3, 6, 14–18, and 20 each require a dummy channel structure filled with a dielectric layer and extending vertically through the conductor/dielectric layer pairs in the memory stack. With respect to the dummy channels recited in limitation 14.E, Petitioner asserts that Nishikawa teaches channel structures and that a person having ordinary skill in the art would have been motivated to include dummy channels, of either the same materials or with a solid dielectric fill, in Nishikawa's memory stack. *See, e.g.*, Pet. 59–64, 82. Petitioner asserts that it was well known to a person having ordinary skill in the art to include dummy channels. *Id.* at 59, 63.[8] Petitioner asserts that a POSITA would have been motivated to add dummy channels to Nishikawa. In particular, Petitioner asserts that adding dummy channels would (1) reduce the likelihood of defective bits on the edge of the memory cell region; (2) result in a more uniform feature pattern so as to reduce processing issues; and (3) in a gate replacement process, provide structural support without consuming space above the structures. *Id.* at 59–63. In its Reply, Petitioner reframes this reason to combine as: "Nishikawa poses edge effect and stability problems, and . . . dummy channels were both a known and suitable option for addressing these problems." Pet. Reply 13.

[8] As acknowledged by Patent Owner, Petitioner does not rely on Nishikawa123 for teaching dummy channels. PO Resp. 35.

Patent Owner first argues that Nishikawa already discloses structures for providing structural support during a gate replacement process. PO Resp. 36–41 (citing Ex. 1005, 10:10–12 ("Separator dielectric structures 45 can provide structural support to the insulating layers 32 after formation of the interlayer cavities")). Patent Owner argues that the separator dielectric structures in Nishikawa are for the same purpose as Petitioner's added dummy channels; i.e., to support recesses caused by loss of sacrificial material during the gate replacement process. PO Resp. 36–37. Patent Owner argues that these separator dielectric structures extend throughout the stack, and that there is no evidence that dummy channels would be helpful, rather than redundant and unnecessary, where such structures already exist in Nishikawa. *Id.* at 39–41 (citing Ex. 2021 ¶¶ 88–89).

In our Institution Decision, we agreed with Patent Owner, stating:

> To the extent that Petitioner's addition of dummy structures would result in additional structural support to Nishikawa's existing separator dielectric structures, Petitioner has not explained how such additional support beyond what Nishikawa discloses, in view of any tradeoffs with additional processing needed to create additional dummy channels, would be viewed as desirable by a person having ordinary skill in the art. Consequently, the record does not support Petitioner's reason to combine dummy channels as known in the art with the teachings of Nishikawa.

Inst. Dec. 20.

We now reach a different determination based upon the post-institution record. In its Reply, Petitioner provides new evidence showing that the use of dummy channels in the contact region was conventional to prevent collapse. Pet. Reply 17–22 (citing Exs. 1022, 1112, 1113, 1114,

1031).[9] For example, Dr. Lee quotes a passage describing the advantages of dummy structures in the staircase structure.

> dummy structures heretofore have not been provided in a stair-like end portion of an array. Accordingly, the floors/ceilings that are vertically between the respective void spaces 29 in FIGS. 9 and 10 may be sagged, bent, or broken during processing due to lack of support. In accordance with one embodiment of the invention, dummy structures in the end portion support the features (e.g., the respective ceilings and floors, or plates) from vertical movement, for example by laterally engaging side portions of such floors/ceilings that were created where such dummy structures extend there-through.

Ex. 1105 ¶ 33 (quoting Ex. 1030, 7:19–35). Dr. Lee's testimony is supported by a reference cited by Patent Owner, which states, "a large staircase means much longer, isolated layers suspended in thin air -- and the possibility of structural collapse" but that "added columns . . . support the structure during the removal of the sacrificial material between the staircase layers" in 3D NAND. Ex. 2034,[10] 2–4. Dr. Campbell also agrees that

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[9] Patent Owner does not contend that Petitioner's focus on the contact region amounts to a new argument not in the Petition. *See* PO Sur-reply 17–19. We note that the Petition included the contact region of Nishikawa as part of its asserted "memory stack," and at least nominally supports Petitioner's contact region arguments in its Reply. Pet. 35–36 (annotated Figure 1 of Nishikawa). Moreover, Patent Owner specifically addressed the Petition's reliance on Kai for providing support structures in the contact region. PO Resp. 53 (citing Ex. 1027).

[10] Ex. 2034 is dated February 2019, which is not prior to the August 2018 effective filing date of the '322 patent. PO Resp. ix; Ex. 2034, 1; Ex. 1001, code (60). However, Patent Owner and Dr. Campbell rely on the same portion of this reference for nearly the same point. PO Resp. 67; Ex. 2021 ¶143 (citing Ex. 2034, 2 ("An additional challenge is posed by the removal, in certain types of 3D NAND, of sacrificial layers in between the 'steps' of the staircase.")). At the least, this indicates that Dr. Campbell and Patent

"dummy structures do provide mechanical support." Ex. 1106, 108:19–20. Based on the record evidence, we agree with Petitioner that some advantage accrues from providing structural support in the staircase of a 3D NAND.

Patent Owner disputes that Nishikawa lacks support structures in its staircase so as to motivate adding structures in the staircase. PO Resp. 36–37. Patent Owner argues that Nishikawa's separator structures "extend *throughout* the entire memory stack," noting that the insulating layers 32 extend into its contact region 300. PO Sur-reply 18. Patent Owner argues that Nishikawa's separator dielectric structures 45 provide structural support to the insulating layers 32. PO Resp. 36–37.

Petitioner argues that Nishikawa's separator dielectric structures only extend through a portion of Nishikawa's device; i.e., a portion of the array. Pet. Reply 16. Dr. Lee attests that Nishikawa has no separator in either its peripheral region 200 or its contact region 300, despite the stack extending into the staircase contact region 300. Ex. 1105 ¶ 32 (citing Ex. 1005, Figs. 1, 16). As evidence, Dr. Lee points to the lack of any discussion of Nishikawa's separator in regions 200 or 300.[11] Ex. 2038, 46:1–4. Dr. Lee attests that both Nishikawa and Nishikawa123 relate to the same memory structure. Ex. 2038, 48:1–8. Dr. Lee further attests that a person having ordinary skill would add dummy channels from the edge of the array through the contact region such that it would not reduce memory density. Ex. 2038, 44:15–51:18 (citing Ex. 1005; Ex. 1027); Pet. Reply 17.

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Owner do not contest the need for support in the staircase during sacrificial layer removal.

[11] Although Dr. Lee also points to the existence of a dielectric pillar 66 in Nishikawa123, we discount that as support because pillars 66 are not stated to be in the contact region, and the Petition did not rely on Nishikawa123 for teaching dummy channels. *See* PO Resp. 36 n.1; Pet. 98.

Petitioner's characterization of Nishikawa is persuasive. Nishikawa states that its separator dielectric structures provide a separation of the alternating stack for inclusion of memory structures 55. Ex. 1005, 8:33–9:38. Patent Owner points to language in Nishikawa that the separator dielectric structures 45 "laterally separate various portions of the alternative stack (32, 42)." PO Sur-reply 18 (citing Ex. 1005, 8:33–35). However, Nishikawa discusses the separator dielectric structures only in the context of the memory openings; e.g., for providing memory openings therebetween. Ex. 1005, 8:57–62, 9:1–6 ("Each separator dielectric structure 45 can extend along the first lateral direction ld1 prior to formation of the memory openings 49, and can be divided into a plurality of separator dielectric structures 45 by formation of the memory openings 49 through portions of the separator dielectric structure 45."). The lack of any disclosure in Nishikawa of separator dielectric structures 45 outside the memory array area region, in view of the coupled purposes of those structures and memory structures 55, sufficiently supports Petitioner's contention that Nishikawa's separator dielectric structures are limited to its memory array region 100 and are not taught to extend into contact region 300.

Patent Owner next disputes that, even were additional dummy structures to be provided, "doing so would introduce significant device performance, cost, and processing disadvantages without offering any advantages." PO Resp. 46 (citing Ex. 2021 ¶ 99; Ex. 1029 ¶ 3). Specifically, Patent Owner points to a need to increase the stack to make space for dummy structures, undesirably resulting in a reduced memory density. *Id.* at 47–49 (citing Ex. 2021 ¶ 100–102; Ex. 2022, 48:10–17, 49:8–14 (Dr. Lee's testimony that "achiev[ing] higher density" is "one of the goal[s] of designing 3D NAND"); Ex. 1003 ¶ 165 (Dr. Lee's testimony that

higher density is more desirably cost effective)). Patent Owner further points to the processing risks inherent in forming channels in a high density array, citing Dr. Campbell's testimony that additional channels results in additional risk of creating a "tapered" channel that fails to penetrate all layers of a stack. *Id.* at 49–50 (citing Ex. 2021 ¶¶ 105–106).

Although each additional channel undoubtedly carries with it the risk of tapering, the record does not reflect any particular drawback to a tapered support column. Ex. 2021 ¶ 105; Ex. 2038, 25:9–17 (discussing difficulties of etching narrow holes as generally limiting memory density in a memory stack). Moreover, Dr. Lee attests that dummy channels added to the staircase region do not reduce the memory density. Ex. 2038, 25:13–17, 49:8–16. Dr. Campbell attests that he "can't make any conclusions" because "the [Nishikawa] reference is not drawn . . . to scale" as to whether "it has lots of empty space or if it doesn't have lots of empty space." Ex. 1106, 113:3–9. As discussed above, creating support structures in the staircase contact region counters the risks that floors and ceilings "may be sagged, bent, or broken during processing due to lack of support." Ex. 1105 (quoting Ex. 1030, 7:19–35). Based on the evidence, we determine that a person having ordinary skill in the art would have chanced an incompletely deep dummy channel in the staircase contact region to lower the overall risk that levels in that region become sagged, bent or broken. Consequently, the record supports Petitioner's reason to combine dummy channels as known in the art with the teachings of Nishikawa.

Finally, Patent Owner argues that the teaching of a dummy channel is solely taken from the knowledge in the art, rather than from Nishikawa or Nishikawa123, which is improper. PO Resp. 35, 55 (referring entirely to its circular TAC-based arguments at PO Resp. 29), 55–58 (arguing that a

dummy channel structure is not "unusually simple"); PO Sur-reply 21. We have dismissed these arguments for the circular TAC, and we dismiss the repeated arguments based upon 35 U.S.C. § 311 and 37 C.F.R. §42.104(b)(4) for the same reasons. *Supra* § II.F.1.b. Further, we determine that Petitioner has sufficiently shown that it was known and conventional to provide dummy channels in the staircase region at the relevant time. Ex. 1105 ¶¶ 33–35 (citing Ex. 1022, Fig. 19C, 28:33–35; Ex. 1112, Fig. 12A, 44:37–40; Ex. 1113, Fig. 13B, 16:38–51; Ex. 1114, Fig. 2, ¶32). As discussed above, in such situations it is permissible in an IPR to rely on background knowledge to supply a missing claim limitation. *See Shockwave Med., Inc.*, 142 F.4th 1371, 1378–79 (Fed. Cir. 2025).

Because Petitioner has sufficiently shown that providing additional support would lead one having ordinary skill in the art to add dummy channels to Nishikawa's memory stack (in its staircase contact region), we need not address Petitioner's alternate reasons based upon edge defects, uniformity of the feature pattern, unconsumed space above the dummy channels, and improvement of the gate replacement process. Pet. 59–60, 63; Pet. Reply 22.

*3. Different lateral dimensions of the TAC (claims 13–16, 20)*

Claim element [14.F] requires a "first diameter of the TAC corresponding to each conductive layer of the conductor/dielectric layer pairs is larger than a second diameter of the TAC corresponding to each dielectric layer of the conductor/dielectric layer pairs." Ex. 1001, 22:22–26. Petitioner relies upon the general knowledge in the art to teach a lateral dimension (diameter) of the conductive/dielectric layer pairs being larger than a second lateral dimension of the conductive/dielectric pairs. Pet. 75 (citing Ex. 1037 ("Cui"); Ex. 1027 ("Kai"); Ex. 1003 ¶¶ 172–175), 82.

Petitioner asserts that it would have been obvious for Nishikawa's TAC to have a ribbed shape by forming recesses in one of the stack layers because it was known in the art to create recesses in conductor/dielectric layers to form a ribbed via cavity. *Id.* (citing Ex. 1031 ("Cui"), Fig. 16A, 26:23–33). Petitioner further asserts that such a ribbed via cavity is advantageous because it creates additional area for the dielectric liner (spacer). *Id.* at 76 (citing Ex. 1003 ¶129).

However, as Patent Owner argues, neither Petitioner nor Dr. Lee explain why this additional area is advantageous. Dr. Lee, in support of the Petition, states only that the additional area creates a longer spacer or liner, which is the same purpose as the lateral recesses in the '322 patent. Ex. 1003 ¶ 173; PO Resp. 65. But a reason to combine should not be obtained solely from the challenged patent. *KSR*, 550 U.S. at 421 ("A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning."); *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358, 1367 (Fed. Cir. 2017) ("[W]e cannot allow hindsight bias to be the thread that stitches together prior art patches into something that is the claimed invention.").

Absent reliance on the rationale in the '322 patent, the rationale advanced in the Petition is insufficient. "[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). The Petition asserts that additional area for an insulating spacer would be advantageous, but does not explain why a person having ordinary skill in the art would find it to be so. Neither Dr. Lee nor Petitioner meaningfully addresses why, absent reliance on the disclosure of the '322

patent, a longer spacer filling the additional space with dielectric material would have been considered to be advantageous.

We further determine that the rationale advanced in the reply is newly raised. We consider Petitioner's "additional liner" argument in its Reply to be a separate argument from its "additional space" assertions in its Petition. *Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (stating that although "the Board walks a fine line when interpreting the scope of a petition and determining what arguments have been fairly presented," the Board is "entitled to deference" on that interpretation). The Petition asserted that "it was known to create lateral recesses" that would "advantageously create[] additional area for the insulating spacer." Pet. 76. Petitioner then asserted that "there are only two options for creating such recesses," either in the gates or the dielectric layers, and that "[b]oth were known and have a common benefit." *Id.* at 77. As attested by Dr. Lee, "the rib regions can be made in the sacrificial or conductive gates . . . [or] in the dielectric layers. Both result in the same additional space." Ex. 1003 ¶173. Dr. Lee's testimony supports the Petition's extra space assertion, not the assertion in the Petitioner's Reply that the extra liner is to prevent electrical short-circuits due to insufficient liner covering the sacrificial gates. Pet. Reply 27–32.

As argued by Patent Owner, neither the Cui nor the Kai reference cited in the Petition particularly addresses any benefit to electrical isolation of the gate layers. PO Resp. 66. Dr. Lee cites to the Cui and Kai references only to support that etching in either region (dielectric or sacrificial/ conductive) was known, not for a common advantage accruing from such recesses. Ex. 1003 ¶ 174. Patent Owner argues that Kai describes "that the recesses are filled with blocking dielectric 52 and a floating gate electrode

54 before tunneling dielectric layer 56 is deposited, not a spacer in a TAC." PO Resp. 66 (citing Ex. 1027, 11:35–39, 12:20–23, 12:47–49, 12:56–61, 13:48–51, Figs. 5C–5G; Ex. 1021 ¶ 140). Further, Cui equated providing recesses in the dielectric layers (which are not argued to provide electrical isolation benefits) with recesses in the gate layers (which are).

Thus, the new arguments in the Reply as to electrical isolation benefits "to avoid short circuits, or . . . to increase leakage current suppression" or to "mitigate . . the capacitive coupling of conductor pairs," were not sufficiently advanced in the Petition. Pet. Reply 28–31. Regardless of whether the Petitioner's Reply has established that "ribbed TACS were extremely well-known" because of those electrical properties (Pet. Reply 29), Petitioner did not, in its Petition, present a sufficient reason why a person having ordinary skill in the art would have found their use obvious in Nishikawa. Petitioner argued that the Petition's "extra space" for the spacer argument was really about a larger insulating spacer. Tr. 24:14–16 ("we thought that the additional space, additional liner, that meant additional isolation, so that meant additional dielectric isolation, right?). However, "[a] petitioner may not rely on a vague, generic, and/or meandering petition and later fault the Board for failing to understand what the petition really meant." *Netflix*, 84 F.4th at 1377.

Alternately, Petitioner asserts that typical prior art etches would result in lateral recesses "in either the dielectric spacers or sacrificial layers." Pet. 74–75 (citing Ex. 1039, 2:59–67). However, Petitioner admits that same reference states that "it is important to have an etching gas which can etch both . . . layers without selectivity" to result in "a smooth sidewall." Pet. 74 (quoting Ex. 1039, 2:59–67). This indicates that etching does not inherently result in lateral recesses, but such occurs only with some prior art etch gases.

Moreover, Petitioner's cited reference explicitly states that a person of ordinary skill in the art would find non-smooth sidewalls created by such gases to be an undesirable result. Ex. 1039, 2:59–67. Thus, Petitioner's assertion that a person having ordinary skill in the art would seek to use etches that would result in the claimed first and second diameters is insufficiently supported.

Because Petitioner has not shown the combined references to teach the claimed diameters of claim 14, Petitioner has not shown, by a reasonable likelihood, that claim 14 would have been obvious over Nishikawa or Nishikawa and Nishikawa123. Claims 15, 16, and 20 depend from claim 14, and claim 13 contains similar lateral dimension limitations. Consequently, we determine that Petitioner has not met its burden to show by a preponderance of the evidence that claims 13–16 and 20 would have been obvious.

*4. Claims 3, 6, 8–10, and 19*

We further determine that Petitioner has sufficiently shown that Nishikawa discloses the remaining limitations of claims 3, 6, 8–10, 15, and 19, which contain the "substantially circular" and/or "dummy channel" but not the TAC lateral dimension limitations.

We agree with Petitioner's assertions against the remaining limitations of independent claims 1 (from which claims 3, 6, and 19 depend), and 8 (from which claims 9 and 10 depend). To the extent limiting, Nishikawa describes a three-dimensional memory device as set forth in limitations 1.PRE[12] and 8.PRE. Ex. 1005, 2:3–3:41; Pet. 34. Nishikawa describes a memory stack comprising alternating conductor/dielectric layers (layers 46

[12] Claim 19 depends from claim 1.

and 32) on substrate 8, as set forth in limitations 1.A/B and 8.A/B. Ex. 1005, Fig. 1, 4:43–56, 6:4–5; Pet. 35–36. Nishikawa further describes a channel structure (memory stack structure 55) extending vertically through the paired layers in the memory stack, as set forth in limitations 1.C and 8.C. Ex. 1005, Fig. 1, 11:33–39; Pet. 36–38. Nishikawa further describes a through array contact (backside contact via structure 76) extending vertically through the conductor/dielectric pairs 46/32 and buried into substrate 8, as set forth in limitations 1.D and 8.D. Ex. 1005, Fig. 1 ; Pet. 39–40; Ex. 1003, 110–11. Nishikawa further describes a slit structure, separator dielectric 45, as set forth in limitation 1.E. We further agree with Petitioner that it would have been obvious for a circular-shaped TAC to retain the surrounding spacer. Pet. 78 (citing Ex. 1003 ¶ 180). Patent Owner does not provide any arguments additional to those made with respect to claim 14. Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 8 would have been obvious over Nishikawa, by itself or with Nishikawa123.

With respect to claim 3, which depends from claim 1 via claim 2 (reciting a peripheral contact outside the memory stack), we agree with Petitioner that Nishikawa describes a silicon oxide for use as channel structure and for insulating layers. Ex. 1005, 6:2–8, 6:49–50, 6:57–59; Pet. 65. Dr. Lee attests that in view of the common use of silicon oxide for dielectric elements, a person having ordinary skill in the art would have understood Nishikawa to disclose silicon dioxide TAC and peripheral contact spacers Ex. 1003 ¶ 153. Based on the record, Petitioner has shown by a preponderance of the evidence that it would have been obvious to a person having ordinary skill in the art for the dielectric layers of the dummy channel, TAC spacer, and peripheral contact spacer to have comprised

silicon oxide. Pet. 65–66. Nishikawa describes peripheral contact via structures 86 (peripheral contact) arranged outside the memory stack and in contact with a peripheral device 20 on the substrate. Ex. 1005, Fig. 1, 4:36–39, 5:30–45, 6:52–54; Pet. 57–58. Consequently, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 3 would have been obvious over Nishikawa, by itself or with Nishikawa123.

Claim 6 depends from claim 1, and further recites "a peripheral contact arranged outside the memory stack and in contact with a peripheral device on the substrate," and "a diameter of the TAC is at least equal to a diameter of the peripheral contact; and a diameter of the dummy channel structure is smaller than each of a diameter of the TAC and a diameter of the peripheral contact." Ex. 1001, 21:14–18. For the TAC diameter, Petitioner relies upon either Nishikawa, or the prior art knowledge evidenced by Nishikawa. Pet. 67–68 (relying on its assertions for [1.D]).

With respect to the TAC and peripheral contacts, Petitioner asserts that it was known to make contacts the same size. Pet. 68. As evidence, Petitioner points to Mushiga's through-array contacts 588, one of which extending through the memory stack and another extending outside the memory stack. *Id.* at 68 (citing Ex. 1012, Fig. 5, 10:31–58). Petitioner also points to Nakajima's "C4" contacts, which are asserted to be a TAC and a peripheral contact, being created by a single hole-creation step and a single set of C4-forming steps. *Id.* at 68–69 (citing Ex. 1009, Fig. 2, 7:5:8–11). Petitioner asserts that it would have been obvious to have made TAC and peripheral contacts the same size to save process time by employing a common process to form both, as shown by Mushiga and Nakajima. *Id.* at 69 (also pointing to Tessariol (Ex. 1036)).

Patent Owner argues that Mushiga does not describe the timing of forming the cavities that become structures 588, and therefore, does not teach that they are made by the same process such that they would be the same size. PO Resp. 71 (citing Ex. 1012, Fig. 5, 10:31–38; Ex. 2021 ¶ 150). Patent Owner argues that Nakajima only discusses forming cavities in its stack, arguing that its description of contacts C4 are in its contact area, not its peripheral area 100d. *Id.* at 71–72 (citing Ex. 1009, 7:35–8:11, 4:49–51, 4:57–60, 3:23–30; Ex. 2021 ¶ 151). Patent Owner also points to Nakajima's description of hole H1 being formed in "the layer stack," not outside. *Id.* at 72–73 (Ex. 1009, 7:37–39, 7:41–43; Ex. 2021 ¶ 152). Patent Owner also argues that Tessariol's holes are both located through the stack. *Id.* at 73 (citing Ex. 1036 ¶ 37; Ex. 2021 ¶ 153). Patent Owner also argues that because Nishikawa's TACs 76 and its peripheral contacts 86 are in different regions of the memory device having different structures, a person having ordinary skill in the art would have used different etch chemistries, and not benefited from Petitioner's asserted advantage of using the same process. *Id.* at 74–75 (Ex. 2021 ¶ 155).

We agree with Patent Owner. Dr. Campbell attests to the different materials in Nishikawa's TAC and peripheral areas. Ex. 2021 ¶ 155. As explained by Dr. Campbell, Nishikawa's peripheral contacts 86 are formed "by etching the dielectric material 38 and planarization dielectric layer 170," whereas Nishikawa's TACs are "formed in openings that etch through the stack of alternating, varying materials." *Id.* (citing Ex. 1005, Fig. 1, 6:8–28, 7:4–15). Dr. Campbell attests that a person having ordinary skill in the art would not have used a common process with common etch chemistries. *Id.* We note that Dr. Lee attests that etching of an alternating stack would "naturally and predictably result in ribbed TAC profiles," which is consistent

with Dr. Campbell's testimony that the etching of the stack would not result in the same structure as etching through a single material (such as the dielectric layer 38 in the peripheral contact area). Ex. 1105 ¶¶ 51, 54. Alternately, Dr. Lee agrees that such recesses could be minimized by a particular etch chemistry; such an etchant has not been asserted to be required for a dielectric-only area. *Id.* ¶¶ 51, 54. Neither Petitioner nor Dr. Lee specifically explains why or how Nishikawa's different regions would use the same contact-forming process so as to be able to gain the asserted advantage of saving process time.

With respect to Petitioner's assertion that it was known in the art to form contacts having the same diameter, Petitioner does not show that this applies specifically to different types of contacts; specifically, that contacts in a peripheral area should have the same diameter as through-array contacts. Dr. Lee relies on the Wolf textbook, but that merely states, "contact holes of identical dimension would need to be used if this problem was not solved." Ex. 1035, 33; Ex. 1003 ¶ 160. Wolf immediately provides the solution: dry etching. Ex. 1035, 33. Thus, Wolf itself teaches that contact holes need not be of the same dimension.

Thus, we determine that Petitioner has not supported its proposed reasons to modify Nishikawa to have identical diameters for its TACs and its peripheral contacts. Consequently, Petitioner has not shown that claim 6 would have been obvious over Nishikawa, by itself or with Nishikawa123.

With respect to claim 9 and its dependent claim 10, Petitioner relies on its same-diameter reasoning set forth for its claim 6 assertions. Pet. 79–81. For the same reasons expressed with respect to claim 6, Petitioner has not shown that claims 9 or 10 would have been obvious over Nishikawa, by itself or with Nishikawa123.

With respect to claim 19, Petitioner relies on its assertions for claim limitation [8.D]. Pet. 83. Patent Owner does not present arguments additional to those presented against limitation [8.D]. For the same reasons expressed above with respect to claim 8, we determine that Petitioner has shown, by a preponderance of the evidence, that claim 19 would have been obvious over Nishikawa, by itself or with Nishikawa123.

*G. Claims 11, 12, 17, and 18 over Nishikawa alone or in combination with Nishikawa123, further in view of Lu*

Petitioner asserts that Lu teaches the "multi-deck" limitations in dependent claims 11, 12, 17, and 18. Pet. 10, 84–88.

Claims 11 depends from claim 8, and claim 12 depends from claim 11. Ex. 1001, 21:49, 53. Patent Owner challenges Petitioner's assertions only based upon arguments previously presented and rejected against claim 8. PO Resp. 76. We have reviewed Petitioner's assertions, including that Lu teaches techniques to form upper and lower memory decks (decks 401, 402), the upper and lower channel structures (channel materials 424, 434), an inter-deck plug (material 437) in view of Lu's teachings that decks increase memory density, and find them persuasive for the reasons stated therein. Pet 84–88. Thus, Petitioner has met its burden to show, by a preponderance of the evidence, that claims 11 and 12 would have been obvious.

Claims 17 and 18 depend from claim 14, for which Petitioner has not met its burden to show obviousness. Petitioner's arguments for claims 17 and 18 do not provide any additional showing that sufficiently demonstrates obviousness of the limitations of claim 14, which are incorporated by dependency into claims 17 and 18. Therefore, Petitioner has not met its

burden to show claims 17 and 18 would have been obvious over its asserted combination of references.

## III. CONCLUSION

For the reasons discussed above, we conclude Petitioner has shown by a preponderance of the evidence that claims 3, 8, 11, 12, and 19 of the '322 patent are unpatentable, and has not shown by a preponderance of the evidence that claims 6, 9, 10, 13–18, and 20 of the '322 patent are unpatentable. Our conclusions are summarized in the table below.

| Claims | 35 U.S.C. § | Reference(s)/ Basis | Claims Shown Unpatentable | Claims Not shown Unpatentable |
|---|---|---|---|---|
| 3, 6, 8–10, 13–16, 19–20 | 103 | Nishikawa | 3, 8, 19 | 6, 9, 10, 13–16, 20 |
| 11, 12, 17, 18 | 103 | Nishikawa, Lu | 11, 12 | 17, 18 |
| 3, 6, 8–10, 13–16, 19–20 | 103 | Nishikawa, Nishikawa123 | 3, 8, 19 | 6, 9, 10, 13–16, 20 |
| 11, 12, 17, 18 | 103 | Nishikawa, Nishikawa123, Lu | 11, 12 | 17, 18 |
| **Overall Outcome** | | | 3, 8, 11, 12, 19 | 6, 9, 10, 13–18, 20 |

## IV. ORDER

For the foregoing reasons, it is:

Accordingly, it is

ORDERED that Petitioner establishes by a preponderance of evidence that challenged claims 3, 8, 11, 12, and 19 are unpatentable; and

ORDERED that Petitioner does not establish by a preponderance of evidence that challenged claims 6, 9, 10, 13–18, and 20 are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.[13]

[13] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), (b)(2).

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