UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01404
Patent 9,147,609 B2

Before HYUN J. JUNG, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges.*

JUNG, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Dismissing Petitioner's Motion to Exclude
37 C.F.R. § 42.64(c)

I. INTRODUCTION

We have jurisdiction under 35 U.S.C. § 6 (2024). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 (2024). For the reasons that follow, we determine that Samsung Electronics Co., Ltd and Samsung Electronics America, Inc. (collectively, "Petitioner") have shown by a preponderance of the evidence that claims 1–18 of U.S. Patent No. 9,147,609 B2 (Ex. 1001, "the '609 patent") are unpatentable. We also dismiss Petitioner's motion to exclude evidence.

A. Background and Summary

Petitioner filed a Petition (Paper 1, "Pet.") requesting institution of an *inter partes* review of claims 1–18 of the '609 patent. Harbor Island Dynamic, LLC ("Patent Owner") filed a Preliminary Response. Paper 7. Pursuant to 35 U.S.C. § 314, we instituted an *inter partes* review of claims 1–18 of the '318 patent on all presented challenges. Paper 9 ("Inst. Dec."), 18.

After institution, Patent Owner filed a Response (Paper 17, "PO Resp."), to which Petitioner filed a Reply (Paper 19, "Pet. Reply"), and Patent Owner, thereafter, filed a Sur-reply (Paper 22, "PO Sur-reply"). Petitioner also filed a motion to exclude evidence (Paper 26), and Patent Owner filed an opposition to the motion (Paper 27). Petitioner subsequently filed a reply to Patent Owner's opposition. Paper 28. An oral hearing in this proceeding was held on January 7, 2026; a transcript of the hearing is included in the record. Paper 31 ("Tr.").

B. Real Parties in Interest

The parties assert that they are the sole real parties in interest. Pet. 82; Paper 5 (Patent Owner's Mandatory Notices), 2.

C. Related Matters

The parties identify *Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.,* Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) as a related matter. Pet. 82; Paper 5, 2.

D. The ’609 Patent (Ex. 1001)

The ’609 patent issued on September 29, 2015, from an application filed on March 8, 2012 and claims priority to a provisional application filed on October 7, 2011. Ex. 1001, codes (22), (45), (60), 1:6–9. Figure 4 of the ’609 patent is reproduced below.

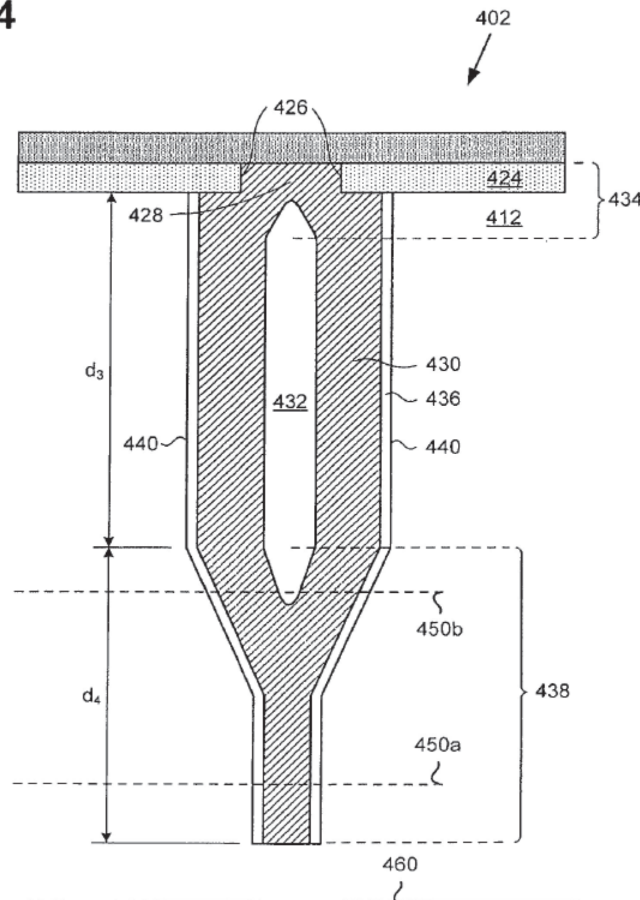


Figure 4 is a “cross-sectional view of a through silicon via within a semiconductor substrate.” Ex. 1001, 2:9–11. Substrate 412 is etched to first depth d_3 to form sidewalls 440 of through silicon via (“TSV”) 402. *Id.* at

4:16–18. A second etch to second depth d_4 is performed so that TSV 402 tapers from first depth d_3 to second depth d_4. *Id.* at 4:22–24. Conductive filler 430 is deposited on sidewalls 440 of TSV 402 "such that hollow center portion 432 and pinched off region 438 are formed in through silicon via 412." *Id.* at 4:47–50.

The tapered portion "allows conductive filler 430 to completely fill the bottom portion of TSV 402." Ex. 1001, 4:50–53. "Hollow center portion 432 provides many beneficial features," such as, reducing the intrinsic inductance of TSV 402 and reducing the thermal and mechanical stress of substrate 412 "by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions." *Id.* at 4:60–66.

E. Illustrative Claim

The '609 patent includes 18 claims, all of which Petitioner challenges. Claim 1, reproduced below, and claim 11 are the independent claims.

> 1. A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:
>
> a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;
>
> a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;
>
> wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said pinched off region.

Ex. 1001, 5:66–6:15.

F. Asserted Prior Art and Proffered Testimonial Evidence

Petitioner identifies the following references as prior art in the asserted grounds of unpatentability:

Name	Reference	Exhibit
Farooq	US 8,327,288 B1, issued Aug. 7, 2012	1016
Cooney	US 2009/0278237 A1, published Nov. 12, 2009	1004
Chen	US 2010/0032843 A1, published Feb. 11, 2010	1011
Dean	US 2011/0057319 A1, published Mar. 10, 2011	1010

Petitioner contends that Cooney and Chen are prior art under §§ 102(a), (b), and (e) and that Farooq and Dean are prior art under §§ 102(a) and (e). Pet. 8–9. Petitioner also provides a Declaration of Dr. Scott E. Thompson, Ph.D. in Support of Petition (Ex. 1002) and a Supplemental Declaration of Scott E. Thompson, Ph.D. (Ex. 1025).

Patent Owner provides a Declaration of Mr. John Berg. Ex. 2012. Patent Owner also filed a deposition transcript for Dr. Thompson. Ex. 2007.

G. Asserted Grounds

Petitioner asserts that claims 1–18 are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1–6, 9–14, 17, 18	102(b)	Cooney
1–6, 9–14, 17, 18	103(a)	Cooney
7, 15	103(a)	Cooney, Dean
8, 16	103(a)	Cooney, Farooq
8, 16	103(a)	Chen, Cooney

Pet. 9.

II. ANALYSIS

A. Petitioner's Motion to Exclude

Petitioner moves to exclude Exhibit 2008 (*Thermal Stresses around Void in Through Silicon Via in 3D SiP*, by T. Kinoshita, et al., published in the 2014 International Conference on Electronics Packaging (April 2014)), Exhibit 2010 (*TSV Cu Filling Failure Modes and Mechanisms Causing the Failures*, by J.W. Choi, et al., published in IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 4 (April 2014)), and Exhibit 2011 (*Low Stress TSV Arrays for High-Density Interconnection*, by Jiao, et al. (2022)). Paper 26, 1. Petitioner asserts that Patent Owner failed to authenticate these exhibits and they are irrelevant, prejudicial, and confusing. *Id.* (citing Fed. R. Evid. 401, 402, 403, 901).

For the reasons stated below, we do not need to rely on these exhibits. We only cite to Exhibit 2008 to indicate where the parties find support for their argument. Accordingly, Petitioner's Motion to Exclude is dismissed as moot.

B. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent [claim] it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). This burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail in an *inter partes* review, the petitioner must support its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

Petitioner contends that the challenged claims of the '609 patent are unpatentable under §§ 102 and 103. Pet. 9. To establish anticipation under

35 U.S.C. § 102, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Each element of the challenged claim must be found, either expressly or inherently, in the single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). When evaluating a prior art reference in the context of anticipation, the reference must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). "[A] reference can anticipate a claim even if it 'd[oes] not expressly spell out' all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would 'at once envisage' the claimed arrangement or combination." *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

A claim is unpatentable under § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). When evaluating a

combination of teachings, we must also "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

C. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art "would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems" and that "[a]dditional relevant work experience can compensate for less education, and *vice versa*." Pet. 9–10 (citing Ex. 1002 ¶¶ 72–74). We preliminarily adopted Petitioner's proposed level of ordinary skill in the art. Inst. Dec. 13.

Patent Owner responds that a person of ordinary skill in the art "would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication." PO Resp. 7. Patent Owner also argues that "[a]dditional formal education (such as Master of Science degrees) would compensate for less technical experience and vice versa." *Id.* (citing Ex. 2012 ¶¶ 22–26).

Patent Owner contends that Petitioner's proposed level of ordinary skill in the art "imposes a requirement of a master's degree," but "engineers working in this field, and implementing designs such as that described in the '609 Patent, typically have bachelor's degrees." PO Resp. 8 (citing Ex. 2012 ¶ 24). Patent Owner, thus, argues that one of ordinary skill in the art would not have needed a master's degree. *Id.* (citing Ex. 2012 ¶ 24).

Petitioner replies that the difference in the parties' proposed level of skill in the art is immaterial. Pet. Reply 1. Petitioner notes that the parties

agree that one of ordinary skill in the art "would have at least two years of experience in semiconductor design and fabrication." *Id.* (citing Pet. 9; PO Resp. 7). Petitioner also argues that Patent Owner "identifies no analysis that would turn on whether a [person of ordinary skill in the art] held a bachelor's or master's degree." *Id.* at 1–2 (citing PO Resp. 7–35). Patent Owner does not provide an argument in reply. *See* PO Sur-reply.

Based on the full record, we maintain and affirm that a person of ordinary skill in the art "would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems" and that "[a]dditional relevant work experience can compensate for less education, and *vice versa*." Pet. 9–10 (citing Ex. 1002 ¶¶ 72–74). We agree with the parties that any differences in the parties' proposed level of ordinary skill would not affect our analysis. Pet. Reply 1; Tr. 25:4–9 (Patent Owner's counsel agreeing that any differences in the parties' proposed level of ordinary skill in the art are immaterial). We also find that Petitioner's proposed level of ordinary skill in the art is consistent with the '609 patent and the asserted prior art.

D. Claim Construction

In an *inter partes* review, the claims are construed

> using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Petitioner contends that "no terms need construction to resolve the controversy in this forum." Pet. 8. We did not need to construe explicitly any claim terms for institution. Inst. Dec. 14.

Patent Owner responds that certain functional limitations cannot be ignored as statements of intended use. PO Resp. 8 (citing Pet. 20, 24–25). Patent Owner, thus, argues that "claim construction disputes exist regarding the terms 'to reduce thermal stress in said semiconductor substrate,' 'to provide space for said conductive filler to expand inward,' and 'to prevent contamination during processing of said semiconductor substrate.'" *Id.*

Patent Owner's arguments and evidence are focused predominantly on the phrase "to reduce thermal stress in said semiconductor." PO Resp. 9–16. Patent Owner refers to the same arguments and evidence for "to provide space for said conductive filler to expand inward" and "to prevent contamination during processing of said semiconductor substrate." *Id.* at 16. The parties also provide reply arguments likewise focused on "to reduce thermal stress in said semiconductor." Pet. Reply 9–14; PO Sur-reply 9–13.

Based on the full record and because Petitioner's anticipation challenge is based on giving these recitations no patentable weight and Petitioner's obviousness challenge is based on the same recitations having patentable weight, we determine that resolving whether to give patentable weight to the recitations "to reduce thermal stress in said semiconductor substrate," "to provide space for said conductive filler to expand inward," and "to prevent contamination during processing of said semiconductor substrate" is not necessary to resolve the parties' dispute. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms that . . . are in controversy, and only to the extent necessary to resolve the controversy.'") (quoting *Vivid Techs., Inc. v.*

Am. Sci. & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999)). Based on the full record, we also determine that express claim interpretation of any other claim term is not necessary. *Id.*

E. Asserted Anticipation by Cooney

1. Cooney (Ex. 1004)

Cooney "relates to enhanced performance through substrate vias within microelectronic substrates." Ex. 1004 ¶ 2. It describes "microelectronic structure, such as a semiconductor structure, and a method for fabricating the microelectronic structure." *Id.* at code (57). Reproduced below is Figure 6 of Cooney.

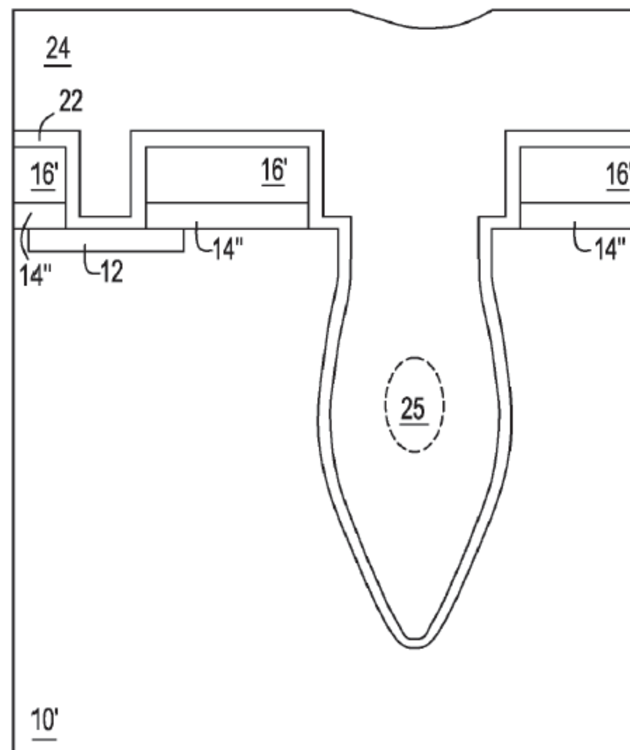


FIG. 6

Figure 6 is one of "a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a microelectronic structure." Ex. 1004 ¶ 23. Semiconductor substrate 10' derived from

substrate 10 includes contact region 12 and can also include semiconductor devices, such as, "resistors, transistors, diodes, and capacitors." *Id.* ¶¶ 26, 32, 42, 63, Figs. 1–4.

Aperture A4 is etched using a photoresist layer as a mask, and "aperture A4 is formed with a downward pointing torpedo shape." Ex. 1004 ¶ 42, Fig. 4. After stripping the photoresist layer, "an extended aperture (i.e., a vertically extended aperture) is formed from the aperture A4" that "includes: (1) a first region R1 that is a first comparatively wide region," "(2) a second region R2 that is a constricted region," "(3) a third region R3 that is a second comparatively wide region," and "(4) a fourth region having a generally but not necessarily pointed inward taper." *Id.* ¶¶ 49, 50, Fig. 5. Wider regions R1, R3 and the inward taper of R4 "in general are intended to provide for ease in filling the extended aperture," and constricted region R2 "is intended to completely seal off any void that may form within third region R3, and to localize that void to the third region R3." *Id.* ¶ 51.

Liner layer 22 is "formed conformally upon the semiconductor substrate" and "incompletely fill[s] the extended aperture." Ex. 1004 ¶ 55, Fig. 6. Conductor layer 24 can have "optional void 25 located therein" or "may be deposited or formed with a void 25." *Id.* ¶¶ 55, 60, Fig. 6. "[V]oid 25 is localized to the second comparatively wide region R3 of the extended aperture." *Id.* ¶ 60.

The semiconductor structure includes through substrate via 24'' that penetrates from front to back of substrate 10''. Ex. 1004 ¶ 65, Fig. 10. Through substrate via 24'' is "formed into an aperture within substrate 10'' . . . that has an irregular sidewall profile." *Id.*

> [T]he irregular sidewall aperture includes: (1) a first comparatively wide region . . . ; (2) a constricted region

> contiguous with and below the first comparatively wide region; (3) a second comparatively wide region contiguous with and below the constricted region; and (4) an inward tapered region contiguous with and below the second comparatively wide region.

Id. "[T]he first comparatively wide region of the aperture aids in efficiently filling the aperture with the through substrate via 24''," and "[t]he constricted region provides for surface closure of any voids that may form in the second comparatively wide region." *Id.* ¶ 66. "The second comparatively wide region, due to the increase in linewidth thereof, provides for ease in filling the aperture," and "the inward tapered region allows for ease in filling at least a bottom portion of the aperture absent forming a void within the via that is filled into the aperture." *Id.*

1. Claim 1

a) "A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:"

Petitioner argues that, if the preamble is limiting, Cooney discloses it. Pet. 15–16 (citing Ex. 1002 ¶¶ 110–111; Ex. 1004 ¶¶ 26, 32, Fig. 1).

We find that the portions of Cooney cited by Petitioner disclose semiconductor substrate 10 "include[s] located and formed therein semiconductor devices that are appropriate for a semiconductor circuit," such as "resistors, transistors, diodes and capacitors." Ex. 1004 ¶¶ 26, 32, Fig. 1. We also credit Petitioner's testimonial evidence regarding the preamble, because Cooney supports it. Ex. 1002 ¶¶ 110–111; Ex. 1004 ¶¶ 26, 32, Fig. 1. Patent Owner does not present a response regarding the preamble. PO Resp. 17–35.

Based on the full record, Petitioner persuades us, and we find, that Cooney discloses the preamble of claim 1. Because we find that Cooney discloses the preamble, we need not determine if the preamble is limiting.

> *b) "a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate"*

Petitioner argues that Cooney discloses the above-quoted limitations. Pet. 16–17 (citing Ex. 1002 ¶¶ 112–115; Ex. 1004 ¶¶ 65, 66, Fig. 10).

We find that the portions of Cooney cited by Petitioner disclose through substrate via 24'' in semiconductor substrate 10'' and show through substrate via 24'' extending from one surface of semiconductor substrate 10'' to an opposite surface. Ex. 1004 ¶¶ 65, 66, Fig. 10. We also credit Petitioner's testimonial evidence that Cooney's substrate 10'' includes a plurality of through substrate vias 24'' and substrate 10'' has top and bottom surfaces between which the through substrate vias extend, because the cited portions of Cooney support it. Ex. 1002 ¶¶ 112–115; Ex. 1004 ¶¶ 65, 66, Fig. 10. Patent Owner does not present a responsive argument regarding the above-quoted limitations. PO Resp. 17–35.

Based on the full record, Petitioner persuades us, and we find, that Cooney discloses "a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate."

> *c) "a conductive filler disposed within each of said plurality of through silicon vias"*

Petitioner argues that Cooney discloses the above-quoted limitations. Pet. 17–18 (citing Ex. 1002 ¶¶ 116–119; Ex. 1004 ¶¶ 55, 59, Fig. 6).

We find that the portions of Cooney cited by Petitioner disclose "liner layer 22 located and formed conformally upon the semiconductor structure,"

"incompletely filling the extended aperture" that forms through substrate via 24'' and "conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture" that forms through substrate via 24''. Ex. 1004 ¶ 55, Fig. 6. We also credit Petitioner's testimonial evidence regarding the recited conductive filler, because the cited portions of Cooney support it. Ex. 1002 ¶¶ 116–119; Ex. 1004 ¶¶ 55, 59, Fig. 6. Patent Owner does not present a responsive argument for the above-quoted limitations. PO Resp. 17–35.

Based on the full record, Petitioner persuades us, and we find, that Cooney's conductor layer 24 discloses "a conductive filler disposed within each of said plurality of through silicon vias."

d) "each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate"

Petitioner argues that Cooney teaches that each of its through silicon vias may have void 25. Pet. 19–20 (citing Ex. 1002 ¶¶ 120–134; Ex. 1004, code (57), ¶¶ 51, 55, 60, Fig. 6). Petitioner also argues with citations to case law that "to reduce thermal stress in said semiconductor substrate" is entitled to no patentable weight, because it states a use or an explanation of the hollow center. *Id.* at 20. Petitioner further argues that "the '609 patent does not identify any features of the hollow center that contribute to thermal stress reduction in the semiconductor substrate." *Id.* (citing Ex. 1002 ¶ 123).

We find that the portions of Cooney cited by Petitioner disclose "an aperture within a substrate," "[i]nto the aperture is located and formed a via" that "may include a through substrate via," and "[t]he structure of the aperture provides for ease in filling the aperture, as well as void isolation within the via." Ex. 1004, code (57), ¶ 55, Fig. 6.

We also find that Petitioner cites portions of Cooney that disclose "conductor layer 24 with an optional void 25 located therein" (Ex. 1004 ¶ 55) and "conductor layer 24 may be deposited or formed with a void 25, but due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture" (*id.* ¶ 60). Petitioner also cites to Figure 6 of Cooney that shows optional void 25 in conductor layer 24.

Cooney explains that an extended aperture is formed from aperture A4 (Ex. 1004 ¶¶ 42, 49, 50, Figs. 4, 5), liner layer 22 is formed conformally and incompletely fills the extended aperture (*id.* ¶ 55, Fig. 6), conductor layer 24 with optional void 25 is formed on liner layer 22 (*id.* ¶ 55, Fig. 6), and further processing leads to forming through substrate via 24'' in substrate 10'' (*id.* ¶¶ 61–65, Figs. 7–10). We credit Petitioner's testimonial evidence regarding the recited through silicon vias having a hollow center, because the cited portions of Cooney support it. Ex. 1002 ¶¶ 120–122; Ex. 1004 ¶¶ 18, 20, 51, 55, 60, 66, Fig. 6.

Patent Owner responds that Cooney does not mention "thermal stress" and does not disclose the purpose of optional void 25. PO Resp. 21. Patent Owner also argues with citations to record evidence that (1) void 25 does not reduce thermal stress in the substrate, (2) all voids cannot be assumed to reduce such thermal stress, and (3) void 25 has not been shown to necessarily reduce thermal stress. *Id.* at 20–26. Patent Owner further argues with citations to the record that Cooney does not provide enough information to determine if void 25 reduces thermal stress, void 25 would not have been large enough to reduce stress, and voids are typically avoided. *Id.* at 26–31. The parties provide reply arguments addressing these issues. Pet. Reply 2–9, 14–20; PO Sur-reply 2–9, 13–18.

Patent Owner does not dispute that Cooney discloses void 25. PO Resp. 5 ("FIG. 6 of *Cooney* shows a 'conductor layer 24 with an **optional void** 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.'"); *see also id.* at 17–34 (not disputing that void 25 discloses "a hollow center"). Patent Owner also provides no response on whether void 25 exists at the end of Cooney's process. Tr. 25:10–15 (Patent Owner's counsel stating that Patent Owner has "no position regarding that, not no dispute, no position"); *see also* Paper 10, 9 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.").

Patent Owner's arguments focus on whether Cooney's void 25 "reduce[s] thermal stress in said semiconductor substrate." *See* PO Resp. 21–31. Petitioner's anticipation challenge, however, gives no patentable weight to the phrase "to reduce thermal stress in said semiconductor substrate," and, thus, does not need to show that Cooney discloses a void "to reduce thermal stress in said semiconductor substrate." Pet. 19–20.

Based on the full record, Petitioner persuades us, and we find, that Cooney discloses "each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate," if no patentable weight is given to the recitation "to reduce thermal stress in said semiconductor substrate." We analyze below Petitioner's obviousness challenge that gives patentable weight to the phrase "to reduce thermal stress in said semiconductor substrate."

e) "said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward"

Petitioner argues that Cooney discloses void 25 being surrounded entirely by conductive layer 24. Pet. 22–24 (citing Ex. 1002 ¶¶ 135–146; Ex. 1004, code (57), ¶¶ 49–55, Figs. 5, 6). Petitioner also argues that the phrase "to provide space for said conductive filler to expand inward" should be given no patentable weight, because "the '609 patent does not identify any features of the hollow center in the TSV that purportedly allows the conductive filler in the TSV to expand inward." *Id.* at 24–25 (citing Ex. 1001; Ex. 1002 ¶ 139). Petitioner further argues that Cooney discloses "provid[ing] space for said conductive filler to expand inward." *Id.* at 25 (citing Ex. 1002 ¶ 139).

We find that the portions of Cooney cited by Petitioner disclose "conductor layer 24 with an optional void 25 located therein." Ex. 1004 ¶ 55, Fig. 6. We also credit Petitioner's testimonial evidence regarding a "hollow center being entirely surrounded by said conductive filler," because Cooney supports it. Ex. 1002 ¶¶ 135–138; Ex. 1004 ¶¶ 51, 55, Figs. 5, 6. We further credit Petitioner's testimonial evidence that one of ordinary skill in the art would have understood that void 25 allows conductor layer 24 to expand inward into void 25. Ex. 1002 ¶ 139.

Patent Owner argues that "to provide space for said conductive filler to expand inward" should be given patentable weight. PO Resp. 16. Patent Owner does not otherwise present a reason why Cooney fails to disclose "said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward." *Id.* at 17–35.

Based on the full record, Petitioner persuades us, and we find, that Cooney discloses "said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward."

f) *"wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate"*

Petitioner argues that Cooney discloses that its through substrate vias have a pinched off region at a bottom portion similar to the pinched off region 438 described by the '609 patent. Pet. 27–31 (citing Ex. 1001, 4:49–50, 5:3–4, Fig. 4; Ex. 1002 ¶¶ 147–164; Ex. 1004, code (57), ¶¶ 42, 49–55, 60, Figs. 5, 6). Petitioner also argues that the phrase "to prevent contamination during processing of said semiconductor substrate" states a use and should be given no patentable weight. *Id.* at 31. Petitioner further argues that "the '609 patent does not identify any features of the pinched off region that contribute to preventing contamination." *Id.* (citing Ex. 1001; Ex. 1002 ¶ 154). Even if the phrase were given patentable weight, Petitioner argues that Cooney's pinched off region would prevent contamination during processing of the semiconductor substrate. *Id.* (citing Ex. 1002 ¶ 154).

We find that the portions of Cooney cited by Petitioner disclose "aperture A4 is formed with a downward pointing torpedo shape" (Ex. 1004 ¶ 42), "the comparatively wide linewidth of the first region R1, the comparatively wide linewidth of the third region R3 and the inward pointed taper of the fourth region R4 in general are intended to provide for ease in filling the extended aperture" (*id.* ¶ 51), and "the constriction within the second region R2 is intended to completely seal off any void that may form

within the third region R3, and to localize that void to the third region R3" (*id.*). Figures 5 and 6 of Cooney also show the "downward pointing torpedo shape" and "the inward pointed taper of the fourth region R4."

We also credit Petitioner's testimonial evidence regarding the above-quoted wherein clause, because the cited portions of Cooney support it. Ex. 1002 ¶¶ 147, 150–153; Ex. 1004, code (57), ¶¶ 18, 20, 51, 55, 60, 66, Figs. 5, 6. We agree with Petitioner's declarant that Cooney's fourth region R4 with its inward pointed taper matches the description of the '609 patent's pinched off region 438. Ex. 1001, 4:49–50, 5:3–4, Fig. 4; Ex. 1002 ¶¶ 148, 149, 152; Ex. 1004 ¶¶ 42, 49–54, Figs. 5, 6.

Patent Owner argues that "to prevent contamination during processing of said semiconductor substrate" should be given patentable weight. PO Resp. 16. Patent Owner does not otherwise present a specific response for the above-quoted wherein clause. *Id.* at 17–35.

Based on the full record, Petitioner persuades us, and we find, that Cooney discloses "wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate," if "to prevent contamination during processing of said semiconductor substrate" is given no patentable weight. We analyze below Petitioner's obviousness challenge that gives patentable weight to the phrase "to prevent contamination during processing of said semiconductor substrate."

g) "wherein said hollow center is tapered in said pinched off region"

Petitioner argues that Cooney discloses the above-quoted limitation. Pet. 34–36 (citing Ex. 1002 ¶¶ 165–172; Ex. 1004 ¶¶ 42, 49–55, 58, 59, Figs. 5, 6). Petitioner also argues that "it was well known in the art that

conformal deposition processes like chemical vapor deposition cause the deposited material to follow the shape of the underlying surface." *Id.* at 36–37 (citing Ex. 1002 ¶¶ 170, 171; Ex. 1008 ¶ 31; Ex. 1009 ¶ 63). Petitioner, thus, argues that one of ordinary skill in the art would have recognized that Cooney's deposition processes "would have caused the deposited layer to take the shape of the underlying surface" and would have recognized that the conductor layer of the void would have taken on a tapered shape similar to the aperture or a tapered shape towards its bottom portion. *Id.* at 37–38 (citing Ex. 1002 ¶ 172; Ex. 1004, Fig. 6).

We find that the portions of Cooney cited by Petitioner disclose an extended aperture with a "downward pointing torpedo shape" (Ex. 1004 ¶¶ 42, 49–54, Fig. 5), liner layer 22 "formed conformally upon the semiconductor structure of FIG. 5" (*id.* ¶ 55) and "deposited . . . using an atomic layer chemical vapor deposition" (*id.* ¶ 58), "conductor layer 24 with an optional void 25 located therein" (*id.* ¶ 55), and conductor layer 24 comprising "a tungsten material" that "is preferably deposited using a chemical vapor deposition method" (*id.* ¶ 59).

We credit Petitioner's testimonial evidence regarding the above-quoted wherein clause, because the cited portions of Cooney support it. Ex. 1002 ¶¶ 165–167; Ex. 1004 ¶¶ 42, 49–55, 58, 59, Fig. 5. The record also supports Petitioner's testimonial evidence that "conformal deposition would cause the deposited material layer to conform to and take the shape of the underlying structure," "chemical vapor deposition of conductor layer 24 in *Cooney*'s aperture would cause the conductor layer 24 to conformally follow the underlying tapered shape of the aperture walls," and "the conformal deposition of conductor layer 24 would cause void 25 to also have a tapered bottom portion to match the tapered shape of the aperture in

the semiconductor substrate 10." Ex. 1002 ¶¶ 168, 169; Ex. 1004, Fig. 6. Patent Owner does not present a response regarding the above-quoted wherein clause. PO Resp. 17–35.

Based on the full record, Petitioner persuades us, and we find, that Cooney discloses "wherein said hollow center is tapered in said pinched off region."

h) Petitioner Shows by a Preponderance of the Evidence that Cooney Anticipates Claim 1

For the reasons above, we find that Cooney discloses each and every element of claim 1 arranged as recited in the claim. Based on the full record, Petitioner persuades us, and we determine, that Cooney anticipates claim 1.

2. Dependent Claims 2–6, 9, and 10

Claims 2–6, 9, and 10 each depend directly from claim 1. Ex. 1001, 6:16–30, 6:38–44. Claim 2 recites "wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias." *Id.* at 6:16–18. Claim 3 recites "wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate." *Id.* at 6:19–22.

Claim 4 recites "wherein said conductive filler comprises a metallic filler," and claim 5 recites "wherein said conductive filler comprises tungsten." Ex. 1001, 6:23–26. Claim 6 recites "wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center." *Id.* at 6:27–30.

Claim 9 recites "further comprising a pinched off region at a top of each of said plurality of through silicon vias," and claim 10 recites "wherein

each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center." Ex. 1001, 6:38–44

Petitioner argues with citations to the record that Cooney anticipates claims 2–6, 9, and 10. Pet. 38–52. We find that the cited portions of Cooney disclose the limitations of these claims. Ex. 1004 ¶¶ 42, 49–55, 59, 60, 63, Figs. 4, 5, 6, 9. We also credit Petitioner's testimonial evidence for these claims, because the cited portions of the record support it. Ex. 1001, 5:4–5, 5:14–16, Fig. 4; Ex. 1002 ¶¶ 173–207; Ex. 1004, code (57), ¶¶ 18, 20, 42, 49–55, 59, 60, 63, 66, Figs. 4, 5, 6, 9; Ex. 1013 (KR 10-2010-0011480, published Feb. 3, 2010) ¶¶ 12, 27–33, Fig. 1h. Patent Owner responds that Cooney does not anticipate any of the challenged claims. PO Resp. 34.

Based on the full record, Petitioner persuades us, and we determine, that Cooney anticipates claims 2–6, 9, and 10.

3. Independent Claim 11

Petitioner argues that Cooney discloses every element of independent claim 11 in the same manner argued for claim 1. Pet. 52 (citing Ex. 1002 ¶¶ 208–212).

a) "A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:"

Petitioner refers to arguments for claim 1 for the preamble of claim 11. Pet. 53 (citing Ex. 1002 ¶ 209). Patent Owner does not present a response regarding the preamble. PO Resp. 17–35.

Based on the full record and for the reasons given above for the preamble of claim 1, Petitioner persuades us, and we find, that Cooney discloses "[a] semiconductor substrate having a plurality of devices."

Ex. 1002 ¶¶ 110–111; Ex. 1004 ¶¶ 26, 32, Fig. 1. We do not need to determine if the preamble of claim 11 is limiting.

> b) *"a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate"*

Petitioner refers to arguments for claim 1 for the above-quoted limitations of claim 11. Pet. 53 (citing Ex. 1002 ¶ 209). Patent Owner does not present a response for these limitations. PO Resp. 17–35.

Based on the full record and for the reasons given above for similar limitations recited by claim 1, Petitioner persuades us, and we find, that Cooney discloses "a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate." Ex. 1002 ¶¶ 112–115; Ex. 1004 ¶¶ 65, 66, Fig. 10.

> c) *"a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate"*

Petitioner refers to arguments for claim 1 for the above-quoted limitations of claim 11. Pet. 53 (citing Ex. 1002 ¶ 209). Patent Owner argues that Cooney does not disclose "a hollow center . . . for reducing thermal stress in said semiconductor substrate" but does not present a response regarding the remainder of the above-quoted limitations. PO Resp. 17–35.

Based on the full record and for the reasons given above for similar limitations recited by claim 1, Petitioner persuades us, and we find, that Cooney discloses "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a

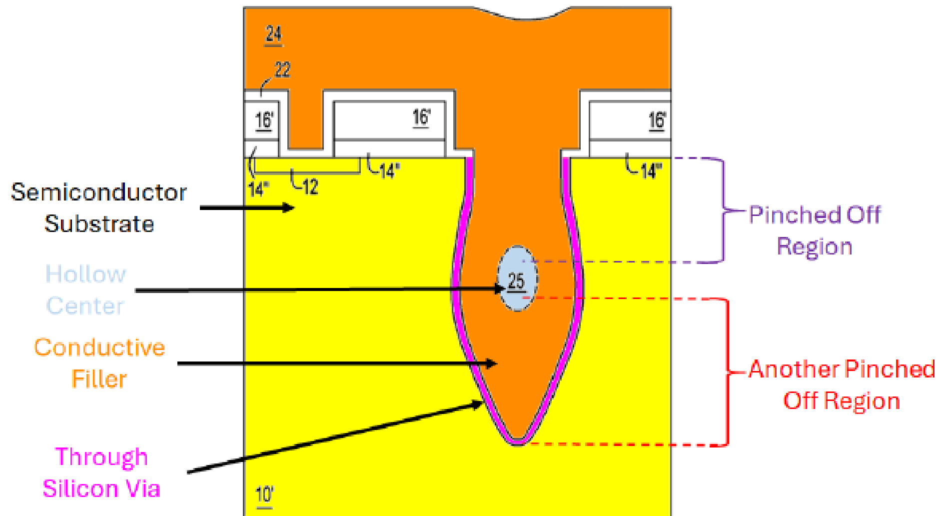
hollow center being entirely surrounded by said conductive filler." Ex. 1004 ¶ 55, Fig. 6. Petitioner also persuades us, and we find, that one of ordinary skill in the art would understand that void 25 of Cooney "provide[s] space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate." Ex. 1002 ¶¶ 139, 209.

Based on the full record, Petitioner persuades us, and we find, that Cooney discloses "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate," if no patentable weight is given to the recitation "for reducing thermal stress in said semiconductor substrate." We analyze below Petitioner's obviousness challenge that gives patentable weight to the phrase "for reducing thermal stress in said semiconductor substrate."

d) "wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region"

Petitioner refers to arguments for claims 1 and 9 for the above-quoted limitations of claim 11. Pet. 53–54 (citing Ex. 1002 ¶¶ 210–211). Petitioner also provides an annotated Figure 6 of Cooney to show pinched off regions at top and bottom portions. *Id.* at 54 (citing Ex. 1002 ¶ 211). Petitioner further argues that Cooney includes a plurality of TSVs, each having pinched off regions. *Id.* (citing Ex. 1002 ¶ 212).

We agree with Petitioner that Figure 6 of Cooney shows pinched off regions at top and bottom portions of its through silicon via. We reproduce below Petitioner's annotated Figure 6.



Cooney, Fig. 6 (annotated).

Figure 6 is a schematic cross-sectional diagram showing the results of a stage in fabricating a microelectronic structure, with Petitioner's labels for "Semiconductor Substrate," "Hollow Center," "Conductive Filler," "Through Silicon Via," "Pinched Off Region," and "Another Pinched Off Region." Pet. 54; Ex. 1004 ¶ 23; *see also id.* ¶¶ 49–55 (describing regions of the extended aperture shown in Figs. 5 and 6). We find that Figure 6 of Cooney shows the above-quoted wherein clauses.

We credit Petitioner's related testimonial evidence because the cited portions of the record support it. Ex. 1001, 5:4–5, 5:14–16, Fig. 4; Ex. 1002 ¶¶ 198–201, 210–212; Ex. 1004, code (57), ¶¶ 18, 20, 42, 49–55, 66, Figs. 5, 6. Patent Owner does not present a response regarding the above-quoted limitations. PO Resp. 17–35.

Based on the full record and for the reasons given above for claims 1 and 9, Petitioner persuades us, and we find, that Cooney discloses "wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion . . . , and wherein said hollow center is tapered in said another pinched off region," if no patentable weight is given to the phrase "to prevent contamination during processing of said semiconductor substrate." We analyze below Petitioner's obviousness challenge that gives patentable weight to the phrase "to prevent contamination during processing of said semiconductor substrate."

e) Petitioner Shows by a Preponderance of the Evidence that Cooney Anticipates Claim 11

For the reasons above, we find that Cooney discloses each and every element of claim 11 arranged as recited in the claim. Based on the full record, Petitioner persuades us, and we determine, that Cooney anticipates claim 11.

4. Dependent Claims 12–14, 17, and 18

Claims 12–14, 17, and 18 each depend directly from claim 11. Ex. 1001, 6:62–7:18. Claim 12 recites "further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias." Ex. 1001, 6:62–67.

Claim 13 recites "wherein said conductive filler comprises a metallic filler," and claim 14 recites "wherein said conductive filler comprises tungsten." Ex. 1001, 7:1–4. Claim 17 recites "wherein said another pinched off region is tapered at said bottom of each of said plurality of through silicon vias," and claim 18 recites "wherein each of said plurality of

through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center." *Id.* at 7:12–18.

Petitioner argues with citations to the record that Cooney anticipates claims 12–14, 17, and 18. Pet. 54–57. We find that the cited portions of Cooney disclose the limitations of these claims. Ex. 1004 ¶¶ 26, 34, 50, 54, Fig. 5. We also credit Petitioner's testimonial evidence for these claims, because the cited portions of the record support it. Ex. 1002 ¶¶ 213–225; Ex. 1004, code (57), ¶¶ 18, 20, 26, 34, 54, 66, Fig. 5. Patent Owner responds that Cooney does not anticipate any of the challenged claims. PO Resp. 34.

Based on the full record, Petitioner persuades us, and we determine, that Cooney anticipates claims 12–14, 17, and 18.

F. Asserted Obviousness Based on Cooney

1. Claim 1

a) "A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising: a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate; a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center . . . , said hollow center being entirely surrounded by said conductive filler . . .; wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion . . . , and wherein said hollow center is tapered in said pinched off region"

For the reasons given above for the anticipation challenge of claim 1 based on Cooney and based on the full record, Petitioner persuades us, and we find, that Cooney teaches or suggests the preamble and the above-quoted limitations of claim 1. Ex. 1002 ¶¶ 110–122, 135–138, 147, 150–153, 165–

167; Ex. 1004, code (57), ¶¶ 26, 32, 42, 49–55, 58–60, 65, 66, Figs. 1, 5, 6, 10.

b) Petitioner's Proposed Modifications

(1) "to reduce thermal stress in said semiconductor substrate"

Petitioner argues that it would have been obvious void 25 similarly reduces thermal stress in the semiconductor substrate based on knowledge in the art that was recognized during prosecution. Pet. 21–22 (citing Ex. 1002 ¶¶ 123–134; Ex. 1005 (U.S. Patent Appl. Publ. No. 2003/0111733 A1 to Pogge et al.) ("Pogge") ¶ 27; Ex. 1006 (U.S. Patent Appl. Publ. No. 2006/0027934 A1 to Edelstein et al.) ("Edelstein") ¶ 47); *see also* Tr. 11:7–11 (Petitioner's counsel confirming that its obviousness argument starts at page 21 of the Petition). Petitioner also argues that there would have been a reasonable expectation of success in including such a void. *Id.* at 22 (citing Ex. 1002 ¶ 134).

(a) Patent Owner's Response

Patent Owner presents the same arguments for both the anticipation challenged based on Cooney and the obviousness challenge based on Cooney. *See* PO Resp. 20–34. As summarized above, Patent Owner responds that Cooney does not mention "thermal stress" and does not disclose the purpose of its "optional void." PO Resp. 21 (citing Ex. 2007, 30:25–31:11). Patent Owner also argues that Petitioner's declarant incorrectly opines that thermal stress is reduced by the presence of Cooney's void 25 and incorrectly assumes that all voids decrease thermal stress in all configurations of TSV's. *Id.* at 20, 21 (citing Pet. 21; Ex. 1002 ¶ 123).

Patent Owner further argues that (1) evidence contradicts Petitioner's assumption that all voids in all TSV's reduce thermal stress in the substrate (*id.* at 22–28), (2) one of ordinary skill in the art would have understood a

void is different from a hollow center that is too small to reduce thermal stress (*id.* at 22, 29–31), and (3) "the torpedo shape used to create *Cooney's* void increases thermal stress by requiring additional metal filler and focusing forces on a smaller part of the silicon, as compared to a typical straight TSV" (*id.* at 22, 28–29).

Specific to the obviousness challenge, Patent Owner responds that the references cited for showing that voids in TSVs were known in the art to reduce thermal stress in the surrounding substrate do not show that voids reduce such thermal stress. PO Resp. 31 (citing Ex. 1002 ¶ 125; Ex. 1005; Ex. 1006; Ex. 2012 ¶¶ 73–77). Patent Owner argues that, although Pogge states that voids relieve stresses due to different thermal coefficients of expansions, Pogge does not state such stresses are borne by the semiconductor substrate and does not teach it was known that all voids decrease thermal stress. *Id.* at 32 (citing Ex. 1005 ¶¶ 26, 27; Ex. 2012 ¶ 74).

Patent Owner also argues that Edelstein is focused on mechanical stresses, not thermal stresses, and never discloses reducing stress in the substrate. PO Resp. 32–33 (citing Ex. 1006 ¶ 47; Ex. 2012 ¶ 75). Patent Owner further argues that Edelstein also does not teach that all voids were known to decrease thermal stress in all TSVs. *Id.* at 33 (citing Ex. 2012 ¶ 75).

According to Patent Owner, Petitioner attempts to create disclosure in the prior art through knowledge in the art, but, even if one of ordinary skill in the art understood that some voids could decrease thermal stress in the surrounding substrate, Petitioner does not provide enough analysis to show that the claims would have been obvious. PO Resp. 33. Regarding Petitioner's argument that it would have been obvious to include a void in Cooney's TSV to reduce thermal stress, Patent Owner argues that Petitioner

fails to show that the particular void in Cooney reduces thermal stress, because Petitioner relies on a flawed assumption that voids in TSVs were known to relieve such stress. *Id.* at 33–34.

(b) Petitioner's Reply

Petitioner replies that Patent Owner incorrectly contends that Pogge does not disclose a void that reduces thermal stress in a semiconductor substrate. Pet. Reply 20 (citing PO Resp. 31, 32). Petitioner argues that one of ordinary skill in the art would have aware of both the disclosure of Pogge and knowledge in the art that voids in a TSV reduce stress induced in the substrate. *Id.* at 20–22. Petitioner also argues that its declarant provided Pogge as an example and cited further to U.S. Patent Application Publication 2010/0171226 A1 to West et al., published July 8, 2010 (Ex. 1024, "West") and U.S. Patent Application Publication 2009/0302480 A1 to Birner et al., published December 10, 2009 (Ex. 1022, "Birner") that both describe a mismatch in the coefficients of thermal expansions of TSV filler material and substrates. *Id.* at 21 (citing Ex. 1002 ¶¶ 47–49, 125–131; Ex. 1022 ¶ 23; Ex. 2007, 26:16–18). In Petitioner's view, one of ordinary skill in the art reading Pogge would have understood the differences in coefficients of thermal expansions would have caused stress in the TSV and the substrate surrounding it. *Id.* at 22 (citing Ex. 1022 ¶ 23; Ex. 1024 ¶ 5; Ex. 1025 ¶¶ 39–41). Petitioner, thus, argues that one of ordinary skill in the art would have understood Pogge to disclose relieving stress in the substrate. *Id.* (citing Ex. 1025 ¶ 41).

Regarding Edelstein, Petitioner replies that one of ordinary skill in the art would have understood that thermal stress is mechanical stress caused by thermal expansion. Pet. Reply 22–23 (citing PO Resp. 32–33; Ex. 1025 ¶ 42). Petitioner argues that Edelstein discloses, and would have been

understood as disclosing, that reducing the mismatch in coefficients of thermal expansions would reduce thermal stress in the substrate. *Id.* at 23 (citing Ex. 1025 ¶¶ 42, 44; Ex. 2008, 2). Petitioner also argues that Edelstein discloses reducing stress in the substrate itself. *Id.* at 24–25 (citing PO Resp. 33; Edelstein ¶¶ 8, 14, 15, 19, 47; Ex. 1025 ¶¶ 45–48).

Petitioner also replies that Patent Owner fails to establish that all voids do not reduce thermal stress in the surrounding substrate. Pet. Reply 15 (citing PO Resp. 32, 33; Ex. 1025 ¶ 49). Petitioner argues that ample evidence shows the known thermal stress relieving behavior of voids. *Id.* Petitioner, thus, argues that it would have been obvious to include a void in Cooney to achieve such stress-relieving benefits, and that Patent Owner fails to present contrary evidence. *Id.* (citing PO Resp. 33–34; Ex. 1002 ¶¶ 125–133; Ex. 1025 ¶ 50). According to Petitioner, "obviousness does not require that all voids decrease thermal stress in all TSVs," just motivation to include voids to decrease thermal stress. *Id.*

(c) Patent Owner's Sur-Reply

Patent Owner replies that "Petitioner does not argue why or how the 'optional void' in *Cooney* would need to be modified in order to reduce thermal stress." PO Sur-reply 18, 19. Patent Owner also argues that Petitioner incorrectly asserts that a void in a TSV was known to reduce thermal stress in the surrounding substrate. *Id.* at 19 (citing Pet. 21). Patent Owner points to the lack of discussion in the Petition regarding how Cooney's void reduces thermal stress. *Id.* (citing Pet. 19–22, 53). Patent Owner also argues that evidence cited for knowledge in the art does not provide a motivation to modify Cooney's void to cause a reduction in thermal stress in the substrate. *Id.*

Patent Owner also replies that Petitioner's evidence shows that some voids decrease thermal stress in the substrate, but some do not. PO Sur-reply 18, 19 (citing PO Resp. 31–33). Patent Owner argues that some voids increase thermal stress. *Id.* at 19 (citing Ex. 2012 ¶¶ 74, 75). Patent Owner, thus, argues that Petitioner insufficiently shows that one of ordinary skill in the art would have understood that all voids, and specifically Cooney's void, reduce thermal stress in the substrate and Petitioner fails to meets its burden to show the claims would have been obvious. *Id.* at 19–20.

(d) Petitioner Shows that One of Ordinary Skill in the Art Would have made the Proposed Modification

For the reasons discussed above for the anticipation challenge, we find that Cooney discloses "silicon vias having a hollow center." Ex. 1002 ¶¶ 120–123; Ex. 1004 ¶¶ 55, 60, Fig. 6. We also find that the portions of Pogge cited by Petitioner show that its "void 25 has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature" (Ex. 1005 ¶ 27) and that the portions of Edelstein cited by Petitioner show that, "[a]lthough it does not change the thermal expansion coefficient, the introduction of a void or voids reduces the effective modulus and Poisson ratio of the through-via, resulting in a compliant through-via that exerts much less stress and force on the surrounding structures" (Ex. 1006 ¶ 47).

As discussed above, we find that Cooney's void 25 is "entirely surrounded by" its conductive filler 24 that, in turn, is surrounded by liner 22 and substrate 10'. Ex. 1004, Fig. 6. We credit Petitioner's relied-upon testimonial evidence that the presence of a void was known to reduce thermal stress in the surrounding substrate, because the citations to the record support it. Ex. 1002 ¶¶ 124–134; Ex. 1005 ¶¶ 1, 9, 25–28, Fig. 2D;

Ex. 1006 ¶¶ 1, 47, 49, Fig. 6F; *see also* PO Sur-reply 19 (acknowledging that "a void *can* decrease thermal stress in the substrate").

We agree with Petitioner's declarant that Pogge provides a void in a TSV similar to Cooney and the '609 patent. Ex. 1001, Fig. 4; Ex. 1002 ¶ 127; Ex. 1004, Fig. 6; Ex. 1005, Fig. 2D. We, thus, credit the testimony that, because of their common structural arrangements, one of ordinary skill in the art would have understood that stress-relieving characteristics in Pogge would have been manifested in Cooney's void. Ex. 1002 ¶ 127.

We also agree with Petitioner's declarant that Edelstein includes a void in a TSV similar to Cooney, the '609 patent, and Pogge. Ex. 1001, Fig. 4; Ex. 1002 ¶ 130; Ex. 1004, Fig. 6; Ex. 1005, Fig. 2F; Ex. 1006, Fig. 6F. We, therefore, credit the testimony that, because of their common structural arrangements, one of ordinary skill in the art would have understood that stress-relieving characteristics in Edelstein would have also been manifested in Cooney's void. Ex. 1002 ¶ 130.

In view of what the full record shows was known in the art, we further agree with Petitioner's declarant that one of ordinary skill in the art "would have understood that voids in TSVs like those of *Edelstein* or *Cooney* would reduce the amount of thermal stress in the substrate generated due to the differences in coefficient of thermal expansion of materials like the conductive filler and the substrate." Ex. 1002 ¶ 130. Particularly, in view of the evidence in Pogge and Edelstein, we agree with Petitioner's declarant that one of ordinary skill in the art "would have been aware of the well-known thermal stress relieving behavior of voids in TSVs filled with conductive materials" and "would have found it obvious that *Cooney*'s TSV with a void enclosed in the conductor layer would also cause a reduction in

the thermal stress in the surrounding substrate consistent with the voids in *Pogge* and *Edelstein*." *Id.* ¶ 131.

We agree with Petitioner's declarant that there would have been a reasonable expectation of success in including a void in Cooney's conductor layer to cause a reduction in thermal stress in the surrounding substrate, because Cooney itself discloses including such a void. Ex. 1002 ¶ 133. Moreover, because the '609 patent itself provides no details regarding how to include a "hollow center to reduce thermal stress in said semiconductor substrate," we determine that the '609 patent indicates that including such a hollow space was within ordinary skill in the art.

Regarding Patent Owner's argument that Cooney lacks disclosure regarding thermal stress (PO Resp. 21), as discussed above, Petitioner provides persuasive argument and evidence that, in view of knowledge in the art, it would have been obvious to include Cooney's void 25 to reduce thermal stress in the surrounding substrate. As for Patent Owner's argument that a void is different from a hollow center and the torpedo shape increases thermal stress (PO Resp. 22, 28–31), Patent Owner does not dispute meaningfully Petitioner's mapping of Cooney's void to the "hollow center" and only disputes that Cooney's void reduces thermal stress (PO Resp. 5, 17–34), and we agree with Petitioner that the claim does not require a particular shape for the recited through silicon via (Pet. Reply 17–18).

Turning to Patent Owner's argument that not all voids reduce thermal stress (PO Resp. 20–28), Petitioner proposes to include Cooney's optional void 25 to reduce thermal stress, and Petitioner's proposed modification does not depend on all voids reducing thermal stress. Pet. Reply 15 (arguing that "obviousness does not require that all voids decrease thermal stress in all TSVs," just motivation to include voids to decrease thermal stress).

Patent Owner's argument and evidence that not all voids reduce thermal stress in the surrounding substrate do not show a deficiency in Petitioner's proposal to include Cooney's void to reduce such stress in view of knowledge in the art evidenced by Pogge and Edelstein. PO Resp. 22–27.

Turning next to Patent Owner's arguments that Pogge does not state thermal stresses relieved by voids are borne by the semiconductor substrate and that Edelstein is focused on mechanical stresses, not thermal stresses, we determine that the full record better supports Petitioner's cited testimonial evidence, not Patent Owner's cited testimonial evidence. Ex. 1002 ¶¶ 124–131, 133; Ex. 1005 ¶ 27; Ex. 1006 ¶ 47; Ex. 1025 ¶¶ 39–50; Ex. 2012 ¶¶ 73–77. We, therefore, give more weight to Petitioner's testimonial evidence regarding Pogge and Edelstein.

Based on the full record, Petitioner persuades us, and we determine, that one of ordinary skill in the art would have modified Cooney to include a void "to reduce thermal stress in said semiconductor substrate" with a reasonable expectation of success.

(2) "to provide space for said conductive filler to expand inward"

Petitioner argues that it would have been obvious to include void 25 to "provide space for said conductive filler to expand inward" because doing so was known in the art. Pet. 25–26 (citing Ex. 1002 ¶¶ 140–145; Ex. 1007 ¶ 36). Petitioner contends that there would have been a reasonable expectation of success. *Id.* at 26 (citing Ex. 1002 ¶ 146).

As discussed above for the anticipation challenge, the full record supports that Cooney has a "hollow center being entirely surrounded by said conductive filler." Ex. 1002 ¶¶ 135–138; Ex. 1004 ¶¶ 51, 55, Figs. 5, 6. We find that Petitioner's citations to the record show that metal was known to

expand into a relatively compliant material that is enclosed by the metal. Ex. 1007 (U.S. Patent Appl. Publ. No. 2011/0304026 A1 to Tsui, published Dec. 15, 2011) ¶ 36. We credit Petitioner's relied-upon testimonial evidence, because the citations to the record support it. Ex. 1002 ¶¶ 140–145; Ex. 1007 ¶¶ 1, 29, 36, 37, 39, 45, 47, Fig. 3. We agree with Petitioner's declarant there would have been a reasonable expectation of success in including a void in Cooney's conductor layer, because Cooney discloses a void in its conductor layer. Ex. 1002 ¶ 145. Patent Owner does not present an argument disputing Petitioner's proposed modification. *See* PO Resp.

Based on the full record, Petitioner persuades us, and we determine, that one of ordinary skill in the art would have modified Cooney to include a void "to provide space for said conductive filler to expand inward" with a reasonable expectation of success. Our determination that one of ordinary skill in the art would have included a void "to provide space for said conductive filler to expand inward" also provides support that the same void would have "reduce[d] thermal stress in said semiconductor substrate" by providing that space for thermal expansion, thereby reducing thermal stress. Ex. 1002 ¶ 143; Ex. 1007 ¶ 36.

(3) "to prevent contamination during processing of said semiconductor substrate"

Petitioner argues that it would have been obvious to include a pinched off region in Cooney to prevent contamination during processing of the semiconductor substrate, because "it was well known that a via closed at both ends prevents contamination of the via during subsequent processes." Pet. 31–32 (citing Ex. 1002 ¶¶ 155–161; Ex. 1013 ¶¶ 12, 27–33, Figs. 1g, 1h). Petitioner also argues that there would have been a reasonable expectation of success in including a pinched off region. *Id.* (citing

Ex. 1002 ¶ 161). Petitioner further argues that Cooney's through substrate vias have no unwanted gaps consistent with the teachings of the '609 patent and, thus, Cooney would have rendered obvious the limitation. *Id.* at 32–34 (citing Ex. 1002 ¶¶ 162–164; Ex. 1004 ¶ 66, Figs. 6, 9).

As discussed above for the anticipation challenge, the full record supports that Cooney's through substrate vias have a pinched off region. Ex. 1002 ¶¶ 147, 150–153; Ex. 1004 ¶¶ 42, 51, Figs. 5, 6. We find that Petitioner's citations to the record show that a via closed at both ends prevented contamination of the via during subsequent processing. Ex. 1013 ¶¶ 12, 27–33, Figs. 1g, 1h. We credit Petitioner's relied-upon testimonial evidence, because the citations to the record support it. Ex. 1002 ¶¶ 155–161, 163, 164; Ex. 1013 ¶¶ 1, 2, 12, 15–18, 22, 27–33, Figs. 1g, 1h. We agree with Petitioner's declarant there would have been a reasonable expectation of success in pinching off Cooney's TSV to prevent contamination during subsequent processing, because Cooney teaches providing pinched-off regions. Ex. 1002 ¶ 161.

We also agree that Cooney's through substrate vias have no gaps consistent with the teachings of the '609 patent. Ex. 1001, 1:45–50; Ex. 1002 ¶¶ 162–164; Ex. 1004 ¶¶ 55, 66, Figs. 9. Patent Owner does not present an argument disputing Petitioner's proposed modification to include pinched off regions in Cooney "to prevent contamination during processing of said semiconductor substrate." *See* PO Resp.

Based on the full record, Petitioner persuades us, and we determine, that one of ordinary skill in the art would have included pinched-off regions "to prevent contamination during processing of said semiconductor substrate" with a reasonable expectation of success.

2. Dependent Claims 2–6, 9, and 10

Claims 2–6, 9, and 10 depend directly from claim 1. Ex. 1001, 6:16–44. Petitioner argues with citations to the record that Cooney would have rendered obvious claims 2–6, 9, and 10. Pet. 38–52. Patent Owner responds that Cooney does not render obvious any of the challenged claims. PO Resp. 34.

Based on the full record and the reasons given above for Petitioner's anticipation challenge, Petitioner persuades us, and we find, that Cooney teaches or suggests the limitations of claims 2–6, 9, and 10. Ex. 1004 ¶¶ 42, 49–55, 59, 60, 63, Figs. 4, 5, 6, 9; Ex. 1002 ¶¶ 173–207.

3. Independent Claim 11

a) "A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising: a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate; a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler . . . , wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion . . . , and wherein said hollow center is tapered in said another pinched off region"

Petitioner argues that Cooney discloses or would have rendered obvious every element of claim 11 in the same manner argued for claim 1 and refers to arguments for claim 1. Pet. 52–53 (citing Ex. 1002 ¶¶ 208–212). Patent Owner does not present a response regarding the above-quoted recitations. PO Resp. 17–35.

For the reasons given above for the anticipation challenge of claims 1 and 11 based on Cooney and based on the full record, Petitioner persuades

us, and we find, that Cooney teaches or suggests the preamble and the above-quoted limitations of claim 11. Ex. 1002 ¶¶ 110–122, 135–138, 147, 150–153, 165–167, 208–212; Ex. 1004, code (57), ¶¶ 26, 32, 42, 49–55, 58–60, 65, 66, Figs. 1, 5, 6, 10.

b) Petitioner's Proposed Modifications

(1) "to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate"

For the reasons given above for Petitioner's modifications proposed for claim 1, Petitioner persuades us, and we determine, that one of ordinary skill in the art would have modified Cooney to include a void "to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate" with a reasonable expectation of success.

(2) "to prevent contamination during processing of said semiconductor substrate"

For the reasons given above for Petitioner's modifications proposed for claim 1, Petitioner persuades us, and we determine, that one of ordinary skill in the art would have modified Cooney to include pinched-off regions "to prevent contamination during processing of said semiconductor substrate" with a reasonable expectation of success.

4. Dependent Claims 12–14, 17, and 18

Claims 12–14, 17, and 18 depend directly from claim 11. Ex. 1001, 6:62–7:18. Petitioner argues with citations to the record that Cooney would have rendered obvious claims 12–14, 17, and 18. Pet. 54–57. Patent Owner responds that Cooney does not render obvious any of the challenged claims. PO Resp. 34.

Based on the full record and for the reasons given above for Petitioner's anticipation challenge, Petitioner persuades us, and we find, that

Cooney teaches or suggests the limitations of claims 12–14, 17, and 18. Ex. 1004 ¶¶ 26, 34, 50, 54, Fig. 5; Ex. 1002 ¶¶ 213–225.

5. Objective Indicia of Nonobviousness

Patent Owner does not present any arguments or evidence regarding any objective indicia of nonobviousness for any of the challenged claims. *See* PO Resp.

6. Petitioner Shows by a Preponderance of the Evidence that Claims 1–6, 9–14, 17, and 18 are Unpatentable

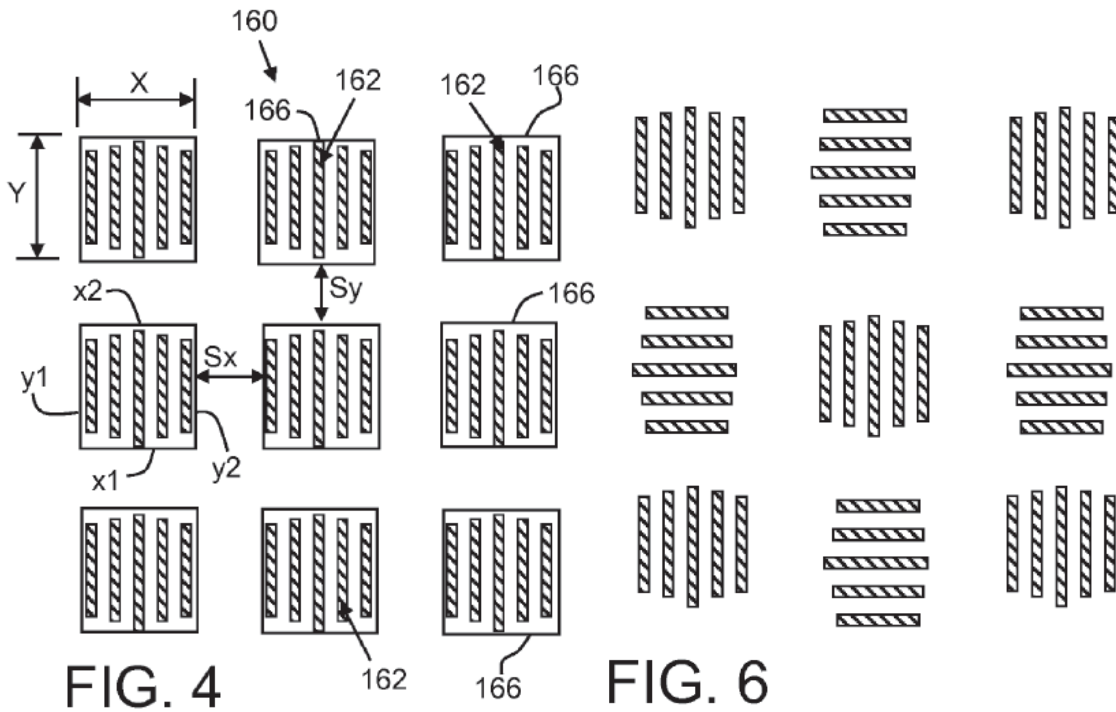
"Once all relevant facts are found, the ultimate legal determination [of obviousness] involves weighing of the fact findings to conclude whether the claimed combination would have been obvious to an ordinary artisan." *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1361 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)). Above, based on the full record before us, we provide our factual findings regarding (1) the level of ordinary skill in the art, (2) the scope and content of the prior art, (3) any differences between the claimed subject matter and the prior art, and (4) objective evidence of nonobviousness.

In particular, we find that (1) Petitioner's proposed level of ordinary skill in the art is consistent with the prior art of record, (2) Cooney teaches or suggests all the limitations of claims 1–6, 9–14, 17, and 18, (3) one of ordinary skill in the art would have modified Cooney in the manner asserted with a reasonable expectation of success, and (4) no objective evidence of nonobviousness has been presented in relation to any of the challenged claims. Weighing these underlying factual determinations, a preponderance of the evidence persuades us that claims 1–6, 9–14, 17, and 18 of the '609 patent are unpatentable over Cooney. *Arctic Cat*, 876 F.3d at 1361.

G. Asserted Obviousness Based on Cooney and Dean

1. Dean (Ex. 1010)

Dean particularly relates "to arranging through silicon vias (TSVs) in an integrated circuit (IC) layout to reduce linearly aligned TSVs." Ex. 1010 ¶ 2. According to Dean, TSVs "are typically elongated vias" and "[i]t has been discovered that when TSVs are aligned they act like perforations making it easy to break a wafer into which they are formed." *Id.* ¶ 17. Dean's method and system, thus, identify linearly aligned TSVs in a portion of an IC layout that includes a plurality of TSVs and modify at least that portion of the IC layout to reduce a number of linearly aligned TSVs. *Id.* at code (57), ¶¶ 5–7, 17. Reproduced below are Figures 4 and 6 of Dean.



Figures 4 and 6 "show a top, schematic views of a portion of a circuit layout illustrating application of the TSV modification system to an array of TSV sets." Ex. 1010 ¶ 14. The circuit layout "includes an array 160 having a substantially uniform periodicity of TSV sets 162 in both the X and Y

directions." *Id.* ¶ 31. "Each TSV set 162 includes all of two or more TSVs therein arranged in a given direction." *Id.* TSV set evaluation rectangle 166 is defined about each TSV set 162, and TSV set evaluation rectangle 166 includes edges x1, x2, y1, and y2. *Id.* Spacing Sy and Sx are calculated between adjacent TSV set evaluation rectangles 166. *Id.*

In another process, TSV set 162 of a selected TSV set evaluation rectangle 166 is rotated to be not aligned with a given direction, such as being substantially perpendicular to the given direction. Ex. 1010 ¶ 33. Dean, thus, "reduces or eliminates wafer breakage by arranging and design rule checking TSVs to avoid alignment, i.e., parallel edges from lining up, and creating high stress points, which cause wafer breakage during IC processing." *Id.* ¶ 39.

2. Claims 7 and 15

Claim 7 depends from claim 1, and claim 15 depends from claim 11. Ex. 1001, 6:31–34, 7:5–8. Both claims recite "wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction." *Id.*

Petitioner argues that Cooney and Dean would have rendered obvious claims 7 and 15. Pet. 66 (citing Ex. 1002 ¶¶ 226–227), 69–70 (citing Ex. 1002 ¶¶ 228–246). In particular, Petitioner argues that Cooney discloses TSVs with "narrow linewidth" that would have been understood to be "a generally narrow elongated shape." *Id.* at 66–67 (citing Ex. 1002 ¶ 228; Ex. 1004 ¶¶ 7, 50). Petitioner also argues that Dean explains that elongated TSVs act like perforations that make a wafer easier to break and discloses rotating a set of vias in a second direction perpendicular to a first direction. *Id.* at 67–69 (citing Ex. 1010 ¶¶ 17, 33, 39, Figs. 4, 6). Petitioner relies on

its testimonial evidence that the directions would correspond to length and width directions. *Id.* at 69 (citing Ex. 1002 ¶ 238).

According to Petitioner, Dean is analogous art. Pet. 60 (citing Ex. 1001, code (57), 1:54–56, 3:1–5, 4:9–5:24; Ex. 1002 ¶ 95; Ex. 1010, code (57), ¶¶ 2, 5–7, 42). Petitioner also argues that both Cooney and Dean are "directed to manufacturing semiconductor substrates with TSVs." *Id.* at 60–61 (citing Ex. 1002 ¶ 239; Ex. 1004 ¶¶ 63, 65, 66; Ex. 1010, code (57), ¶¶ 1, 2, 17, Fig. 4).

Petitioner argues that one of ordinary skill in the art would have been motivated to combine Cooney's manufacturing process with Dean's arrangement of TSVs, because Cooney's TSVs would have been understood to be elongated TSVs aligned with each other that act like perforations on a wafer and Dean teaches using alternating elongated TSVs to reduce wafer breakage. Pet. 60 (citing Ex. 1002 ¶¶ 227–246), 61–64 (citing Ex. 1002 ¶¶ 233–236, 240, 241; Ex. 1004 ¶¶ 7, 17, 50; Ex. 1010 ¶¶ 31, 33, 39, Fig. 6). Petitioner also argues that wafer breakage can cause significant economic losses, wafer contamination from debris generated by wafer breakage, affect manufacturing time, and increase manufacturing cost. *Id.* at 64 (citing Ex. 1002 ¶ 242; Ex. 1010 ¶ 17). Petitioner further argues that Dean teaches it was known to orient elongated TSVs in different directions to reduce wafer breakage. *Id.* at 65 (citing Ex. 1002 ¶ 243). Petitioner additionally argues that the proposed combination "would have involved nothing more than the use of a known technique—lengthwise and widthwise orientation of elongated TSVs—to improve a similar device—*Cooney*'s semiconductor substrate—in the same way." *Id.*

Petitioner also argues that there would have been a reasonable expectation of success, because the proposed combination would have been

well within ordinary skill in the art, would have been a simple implementation of TSV arrangements, and would have merely required combining well-known elements according to known methods. Pet. 65–66 (citing Ex. 1002 ¶¶ 244, 245).

We find that the portions of Cooney and Dean cited by Petitioner teach or suggest the limitations of claims 7 and 15. Ex. 1004 ¶¶ 7, 50; Ex. 1010 ¶¶ 17, 33, 39, Figs. 4, 6. We also credit Petitioner's testimonial evidence for these claims, because the cited portions of the record support it. Ex. 1002 ¶¶ 226–238; Ex. 1004 ¶¶ 7, 42–60; Ex. 1010 ¶¶ 17, 31, 39, Figs. 4, 6. We further credit the testimony that one of ordinary skill in the art would have combined Cooney and Dean in the manner asserted with a reasonable expectation of success. Ex. 1002 ¶¶ 239–246.

Patent Owner responds that that the challenge based on Cooney and Dean explicitly relies on the flawed analysis of the anticipation challenge based on Cooney, does not overcome the deficiencies, and, thus, fails. PO Resp. 34 (citing Pet. 57–70; Ex. 2012 ¶ 77). Petitioner replies that Patent Owner does not contest that Dean discloses the additional limitations of claims 7 and 15, and that Patent Owner's arguments for Cooney fail. Pet. Reply 26. Patent Owner replies that "[t]he remaining grounds all fail because *Cooney* does not anticipate or render obvious either Claim 1 or Claim 11 due to its failure to disclose the reduction of thermal stress in the substrate." PO Sur-reply 20.

Based on the full record, we find that Cooney and Dean teach or suggest the limitations of claims 7 and 15 and that one of ordinary skill in the art would have combined the references in the manner asserted with a reasonable expectation of success. Weighing the underlying factual determinations, a preponderance of the evidence persuades us that claims 7

and 15 of the ’609 patent are unpatentable over Cooney and Dean. *Arctic Cat*, 876 F.3d at 1361.

H. Asserted Obviousness Based on Cooney and Farooq

1. Farooq (Ex. 1016)

Farooq relates “specifically to design and layout of through-silicon via (TSV) structures allowing for enhanced electromigration resistance.” Ex. 1016, 1:8–10. According to Farooq, “[a] traditional TSV cross-section 202 is substantially circular, causing current to travel into or out of metallization layer 204 at the leading edge 206 of TSV cross-section 202 due to low resistance in the TSV structure.” *Id.* at 4:17–20. Farooq also states that “[w]ith almost all current traveling through leading edge 206, it may form a void, which will grow over time, eventually cutting off this area of contact.” *Id.* at 4:20–23.

“By providing a flat edge in the TSV structure where current enters and exits, such as a truncated square cross-section 210 or octagonal cross-section 214, the current is evenly distributed over the length of the edge, as shown in flat edge 212 of the truncated square cross-section 210 and flat edge 216, of octagonal cross-section 214.” Ex. 1016, 4:29–34. “Although in all embodiments, corners are introduced into the design, in the preferred embodiment, the etch process rounds these corners, keeping the local stresses low.” *Id.* at 4:44–46.

2. Claims 8 and 16

Claim 8 depends from claim 1, and claim 16 depends from claim 11. Ex. 1001, 6:35–37, 7:9–11. Both claims recite “wherein each of said plurality of through silicon vias has at least one chamfered corner.” *Id.*

Petitioner argues that Cooney and Farooq would have rendered obvious claims 8 and 16. Pet. 74 (citing Ex. 1002 ¶¶ 248–254). In

particular, Petitioner argues that Farooq discloses truncated corners that evenly distribute current over the length of an edge. *Id.* (citing Ex. 1016, 4:29–34). Petitioner also argues that fabricating Cooney's through substrate vias with flat edges and Farooq's truncated corners would result in through substrate vias with chamfered corners. *Id.* (citing Ex. 1016, 4:29–34, 6:4–19).

According to Petitioner, Farooq is analogous art. Pet. 71 (citing Ex. 1001, code (57), 1:54–56, 3:1–5, 4:9–5:24; Ex. 1002 ¶¶ 101–105; Ex. 1016, 1:18–37, 5:6–12, 6:4–19). Petitioner argues that one of ordinary skill in the art would have been motivated to combine Cooney and Farooq "to ensure uniform current densities along any of the edges where current may flow," and the proposed combination "would have less peak current density," "minimiz[e] current crowding," and "reduce stress at the corners." Pet. 71–72 (citing Ex. 1002 ¶¶ 248–254; Ex. 1016, 4:2–5, 4:17–23, 4:44–46, 6:20–25, Fig. 3; Ex. 1014, 561).

Petitioner further argues that there would have been a reasonable expectation of success, because the proposed combination would have been well within ordinary skill in the art, "a simple implementation of the TSV shape," and "merely require[d] combining well-known prior elements according to known methods." Pet. 73–74 (citing Ex. 1002 ¶ 253).

We find that the portions of Cooney and Farooq cited by Petitioner teach or suggest the limitations of claims 8 and 16. Ex. 1016, 4:29–34, 6:4–19. We also credit Petitioner's testimonial evidence for these claims, because the cited portions of the record support it. Ex. 1002 ¶¶ 247–251; Ex. 1004 ¶¶ 7, 42–60; Ex. 1016, code (57), 1:62–2:5, 3:65–4:5, 4:10–26, 4:29–34, 5:15–17, 5:40–42, 6:4–25, Fig. 3; Ex. 1014, 561. We further credit the testimony that one of ordinary skill in the art would have combined

Cooney and Farooq in the manner asserted with a reasonable expectation of success. Ex. 1002 ¶¶ 251–254; Ex. 1016, 4:29–34, 6:4–19.

Patent Owner responds that the challenge based on Cooney and Farooq does not overcome the deficiencies of the anticipation challenge based on Cooney and, thus, the challenge fails. PO Resp. 34 (citing Pet. 70–74; Ex. 2012 ¶ 77). Petitioner replies that Patent Owner does not contest that Farooq discloses the additional limitations of claims 8 and 16, and that Patent Owner's arguments for Cooney fail. Pet. Reply 26. Patent Owner replies that "[t]he remaining grounds all fail because *Cooney* does not anticipate or render obvious either Claim 1 or Claim 11 due to its failure to disclose the reduction of thermal stress in the substrate." PO Sur-reply 20.

Based on the full record, we find that Cooney and Farooq teach or suggest the limitations of claims 8 and 16 and that one of ordinary skill in the art would have combined the references in the manner asserted with a reasonable expectation of success. Weighing the underlying factual determinations, a preponderance of the evidence persuades us that claims 8 and 16 of the '609 patent are unpatentable over Cooney and Farooq. *Arctic Cat*, 876 F.3d at 1361.

I. Asserted Obviousness Based on Chen and Cooney

1. Chen (Ex. 1011)

Chen relates "particularly to a system and manufacturing through silicon vias." Ex. 1011 ¶ 1. Chen provides "a structure and method for forming through silicon vias beneath an under bump metallization layer" ("UBM"). *Id.* ¶ 5. The UBM can be formed in an octagonal shape. *Id.* ¶ 42. According to Chen, by placing connection TSVs and port TSVs under a UBM, trace lines take up less space on a surface of a die, and, thus, the "die may be spaced closer together and have less of an overall footprint when

connected." *Id.* ¶ 44. "This helps to reduce the size of circuit components in general, leading to smaller devices overall." *Id.*

2. Claims 8 and 16

Petitioner argues that Chen and Cooney would have rendered obvious claims 8 and 16. Pet. 79 (citing Ex. 1002 ¶¶ 255–263), 79–80 (citing Ex. 1002 ¶ 259), 80 (citing Ex. 1002 ¶¶ 258–263). In particular, Petitioner argues that Chen discloses forming TSVs "to reduce the total real estate taken on the surface of a semiconductor die." *Id.* (citing Ex. 1011 ¶¶ 4, 41, Fig. 8B). Petitioner also argues that Chen shows TSVs with chamfered corners. *Id.* at 80 (citing Ex. 1011 ¶ 42, Fig. 8B). Petitioner further argues that using such TSVs "was well known in the art to help minimize electromigration of the conductive material in the TSVs." *Id.* (citing Ex. 1002 ¶ 258).

According to Petitioner, Chen is analogous art. Pet. 76 (citing Ex. 1001, code (57), 1:54–56, 3:1–5, 4:9–5:24; Ex. 1002 ¶¶ 96–100; Ex. 1011, code (57), ¶¶ 1, 6–8, 24–27). Petitioner contends that both Chen and Cooney relate to manufacturing semiconductor substrates with TSVs. *Id.* at 76–77 (citing Ex. 1002 ¶ 259; Ex. 1004 ¶ 18; Ex. 1011 ¶ 1, Fig. 8B).

Petitioner argues that one of ordinary skill in the art would have been motivated to combine the TSV's of Chen with the aperture and sidewall profile of Cooney to aid in filing TSV apertures and to localize any void within the TSV. Pet. 77–78 (citing Ex. 1002 ¶ 261; Ex. 1004 ¶¶ 17, 18, 60, 66). Petitioner also argues that the proposed combination "would have involved nothing more than the use of a known technique—using a particular sidewall profile for the TSVs—to improve a similar device—*Chen*'s TSV—in the same way, namely, to provide ease of filling the via and optimally localizing the void in the TSVs." *Id.* at 78 (citing Ex. 1002 ¶ 261).

Petitioner further argues that there would have been a reasonable expectation of success, because the proposed combination "would have involved a simple geometric design that would have been well within the skill of a [person of ordinary skill in the art]," "would have been a simple implementation of the TSV shape of *Cooney* in *Chen*," and "merely requires combining well-known prior art elements according to known methods." Pet. 78.

We find that the portions of Chen and Cooney cited by Petitioner teach or suggest the limitations of claims 8 and 16. Ex. 1011 ¶¶ 4, 41, 42, Fig. 8B. We also credit Petitioner's testimonial evidence for these claims, because the cited portions of the record support it. Ex. 1002 ¶¶ 255–260; Ex. 1004 ¶ 18; Ex. 1011 ¶¶ 1–4, 41, 42, 44, Fig. 8B; Ex. 1016, 1:62–2:3, 2:29–32, 3:65–4:5, 4:9, 4:29–43. We further credit the testimony that one of ordinary skill in the art would have combined Chen and Cooney in the manner asserted with a reasonable expectation of success. Ex. 1002 ¶¶ 261–263; Ex. 1004 ¶¶ 17, 18, 60, 66.

Patent Owner responds that the challenge based on Chen does not overcome the deficiencies of Cooney. PO Resp. 35 (citing Pet. 74–80; Ex. 2012 ¶ 77). Petitioner replies that Patent Owner does not contest that Chen discloses the additional limitations of claims 8 and 16 and that Patent Owner's arguments for Cooney fail. Pet. Reply 26. Patent Owner replies that "[t]he remaining grounds all fail because *Cooney* does not anticipate or render obvious either Claim 1 or Claim 11 due to its failure to disclose the reduction of thermal stress in the substrate." PO Sur-reply 20.

Based on the full record, we find that Chen and Cooney teach or suggest the limitations of claims 8 and 16 and that one of ordinary skill in the art would have combined the references in the manner asserted with a

reasonable expectation of success. Weighing the underlying factual determinations, a preponderance of the evidence persuades us that claims 8 and 16 of the ’609 patent are unpatentable over Chen and Cooney. *Arctic Cat*, 876 F.3d at 1361.

III. CONCLUSION[1]

Claims	**35 U.S.C. §**	**References/Basis**	**Claims Shown Unpatentable**	**Claims Not Shown Unpatentable**
1–6, 9–14, 17, 18	102(b)	Cooney	1–6, 9–14, 17, 18	
1–6, 9–14, 17, 18	103(a)	Cooney	1–6, 9–14, 17, 18	
7, 15	103(a)	Cooney, Dean	7, 15	
8, 16	103(a)	Cooney, Farooq	8, 16	
8, 16	103(a)	Cooney, Chen	8, 16	
Overall Outcome			1–18	

[1] Should Patent Owner wish to pursue amendment of the challenged claim in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–18 of U.S. Patent No. 9,147,609 B2 have been shown, by a preponderance of the evidence, to be unpatentable;

FURTHER ORDERED that Petitioner's motion to exclude evidence (Paper 26) is dismissed; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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