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Paper 65
Date: February 17, 2026

PUBLIC VERSION

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

OPTRONIC SCIENCES LLC,
Patent Owner.

IPR2024-01132
Patent 7,586,121 B2

Before THU A. DANG, BENJAMIN D. M. WOOD, and KEVIN W. CHERRY, *Administrative Patent Judges.*

CHERRY, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

BOE Technology Group Co., Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1–7 ("the challenged claims") of U.S. Patent 7,586,121 B2 (Ex. 1001, "the '121 patent"). Optronic Sciences LLC ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp."). We instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 14 ("Inst. Dec.").

During the trial, Patent Owner filed a Response (Paper 25, "PO Resp."), Petitioner filed a Reply (Paper 30, "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 33, "PO Sur-Reply").

Both parties requested supplemental briefing to submit what they contended were inconsistent positions taken by each other in the related district court litigation. *See* Ex. 1026 (Transcript of Oct. 8, 2025 teleconference). We authorized the parties' requests for additional briefing. Patent Owner submitted a brief regarding allegedly inconsistent statements by Petitioner (Paper 40, "PO Supp. Br.") and Petitioner submitted a response (Paper 43, "Pet. Supp. Resp."). Petitioner submitted a brief regarding allegedly inconsistent statements by Patent Owner's expert (Paper 41, "Pet. Supp. Br.") and Patent Owner submitted a response (Paper 46, "PO Supp. Resp.").

Petitioner and Patent Owner requested oral argument (Papers 31 and 32). A hearing was conducted on November 18, 2025. Paper 59 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). Having reviewed the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that the challenged claims are unpatentable.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies itself, BOE Technology Group Co. Ltd., as real parties in interest. Pet. 55. Patent Owner identifies itself as the real party in interest. Paper 4, 1; Paper 6, 1.

B. *Related Matters*

Petitioner and Patent Owner state that the '121 patent is asserted in the following litigation: *Optronic Sciences LLC v. BOE Technology Group Co., Ltd.*, 2:23-cv-00549 (E.D. Tex.). Pet. 55; Paper 4, 1; Paper 6, 1. The district court case remains pending. Patent Owner also identifies: *Optronic Sciences LLC v. BOE Technology Group Co., Ltd.*, 2:24-cv-00577 (E.D. Tex.) and *Paneltouch Techs., LLC v. BOE Technology Group Co. Ltd.*, 2:25-cv-00245 (E.D. Tex.). Paper 58, 1.

Patent Owner identifies the following *inter partes* review proceedings between the parties as concerning other patents that may affect or be affected by a decision in this proceeding: IPR2024-01130 (U.S. Patent No. 7,168,842), IPR2024-01131 (U.S. Patent No. 7,226,801), IPR2024-01133 (U.S. Patent No. 9,263,509), IPR2024-01134 (U.S. Patent No. 9,406,733), IPR2024-01135 (U.S. Patent No. 8,158,477), IPR2024-01315 (Patent 8,158,477), IPR2025-00238 (U.S. Patent No. 8,604,471), IPR2025-00239 (U.S. Patent No. 8,502,757), IPR2025-01245 (U.S. Patent No. 9,250,758), IPR2025-01246 (U.S. Patent No. 8,803,836), IPR2025-01267 (U.S. Patent No. 11,260,025), IPR2025-01482 (U.S. Patent No. 8,704,762), IPR2025-01483 (U.S. Patent No. 9,507,477). Paper 58, 1.

C. *The ’121 Patent (Ex. 1001)*

The ’121 patent is titled “Electroluminescence Device Having Stacked Capacitors.” Ex. 1001, code (54). The ’121 patent concerns storage capacitors in electroluminescent (EL) devices. *Id.* at1:6–9. The ’121 patent states that known EL devices typically include thin film transistors (TFTs) and light emitting diodes (LEDs) that may contain organic material and emit light when current is passed through them. *Id.* at 1:13–21. In a current or voltage driven active-matrix organic light emitting diode (OLED) device or polymer light emitting diode (PLED) device, each pixel comprises a set of sub-pixels that include a switching transistor, driving transistor and a storage capacitor. *Id.* at 1:22–27. Noting that a large capacitance avoids grey scale fading, the ’121 patent seeks to provide an improved storage capacitance in a limited area. *Id.* at 1:27–37.

The ’121 patent discloses an EL device may include an array of pixels formed on a substrate, e.g., glass, with each pixel formed in a respective pixel area. *Id.* at 1:41–45, 4:36–37. Figure 1 of the ’121 patent, reproduced below, is a circuit diagram of a pixel of such an EL device. *Id.* at 3:62–64.

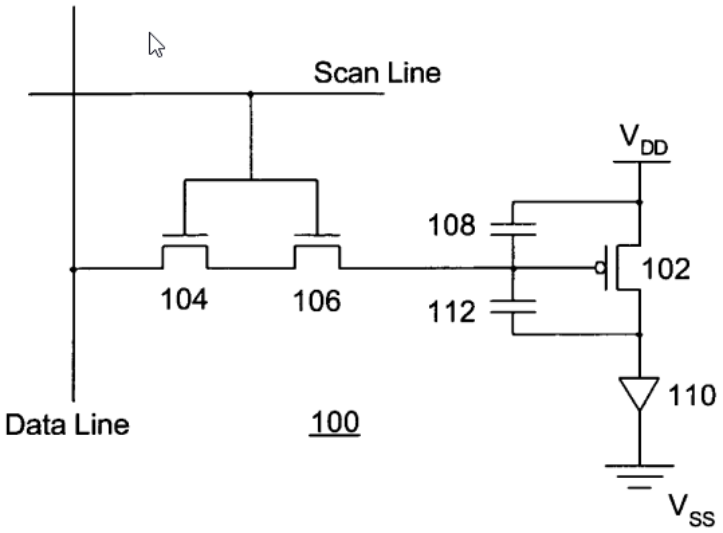


Fig. 1

Ex. 1001, Fig. 1. Transistor 102 is a p-type MOS transistor and transistors 104, 106 are n-type MOS transistors. *See id.* at 4:36–49. The anode of OLED 110 is coupled to the drain of transistor 102 and the cathode is coupled to Vss, which may be ground. As capacitors 108 and 112 hold a charge when transistors 104 and 106 are turned off, in this condition they effectively act in parallel to form a storage capacitor, whose capacitance equals the sum of the individual capacitances, that maintains the gate voltage of transistor 102 for driving OLED 102. *Id.* at 4:60–5:4. By forming capacitor 112 over the same area where capacitance 108 is formed, the storage capacitance is increased without consuming additional chip area and without requiring additional masks. *Id.* at 5:5–11. Figure 2 of the '121 patent, reproduced below, is a cross-sectional view of a part of pixel 100. *Id.* at 3:65–67, 5:12–16.

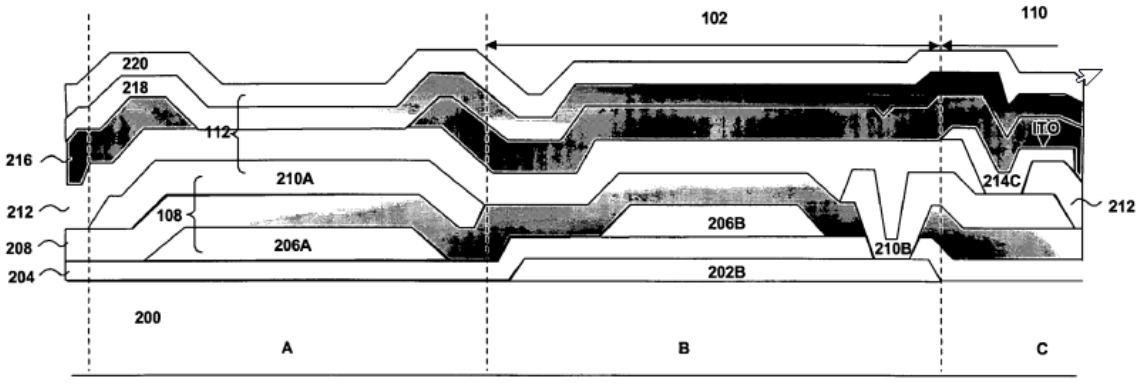


Fig. 2

Ex. 1001, Fig. 2. In Figure 2, part of pixel 100 is shown with capacitors 108, 112 formed over area A, a portion of transistor 102 formed over area B, and gate oxide layer 204 formed over all of area A, B, and C; transistors 104 and 106 are not shown. *Id.* at 5:13–21. Over area A first metal pattern 206A, interlayer dielectric (ILD) layer 208 and second metal pattern 210A collectively form capacitor 108. *Id.* at 5:47–48. Second metal pattern 210A, SiN passivation 212, organic 218, and third metal 220 collectively form capacitor 112. *Id.* at 5:48–50.[1] Over area B, polysilicon pattern 202B provides the source and drain of transistor 102 and first metal pattern 206B serves as the gate of transistor 102. *Id.* at 5:50–53. Over area C, indium tin oxide (ITO) pattern 214C, capping SiN 216, organic 218 and third metal 220 collectively form part of OLED 110. *Id.* at 5:53–55.

D. *Challenged Claims*

Petitioner challenges claims 1–7. Pet. 1. Of the challenged claims, claims 1 and 14 are independent. Claim 1, reproduced below with

[1] Ex. 1001, 5:50 appears to have a typographical error: "capacitor 110" should read --capacitor 112--; reference designator 110 refers to the OLED.

Petitioner's identifiers for the claim limitations, is illustrative of the claimed subject matter.

[1.pre] An electroluminescence (EL) device comprising:

[1.a] a substrate; and

[1.b] a plurality of pixels formed on the substrate, each pixel being in a respective pixel area, each pixel area including at least a first area, a second area, and a third area, where each pixel includes:

[1.c] at least a first capacitor and a second capacitor in the first area, the first capacitor including a first conductive layer formed over a first gate oxide layer, a first dielectric layer over the first conductive layer, and a second conductive layer over the first dielectric layer, and the second capacitor including the second conductive layer, a second dielectric layer over the second conductive layer, and a third conductive layer over the second dielectric layer;

[1.d] a transistor in the second area, the transistor including a first semiconductor layer formed on the substrate, the first gate oxide layer over the first semiconductor layer, and a fourth conductive layer over the first gate oxide layer, wherein the fourth conductive layer is formed of the same conductive film as the first conductive layer, and wherein both the first conductive layer and the fourth conductive layer are directly formed on the gate oxide layer; and

[1.e] a light emitting device in the third area, the light emitting device including a fifth conductive layer, a first organic layer over the fifth conductive layer, and a sixth conductive layer over the first organic layer, wherein the sixth conductive layer is formed of the same conductive film as the third conductive layer.

Ex. 1001, 8:24–54.

E. *Asserted Grounds*

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §[2]	Reference(s)/Basis
1–3, 5	102(e)	Anzai[3]
4	103(a)	Anzai, Yamazaki[4]
1–7	103(a)	Yamazaki, Anzai

Petitioner submits its Petition with the Declaration of Dr. Dean Neikirk (Ex. 1002, "Neikirk Decl."), and its Reply with the Declaration of Dr. Dean Neikirk in Support of Petitioner's Reply (Ex. 1020, "Neikirk Reply Decl.").

Patent Owner supports its contentions with the Declaration of Eric Bretschneider, Ph.D. (Ex. 2005, "Bretschneider Decl.").

III. ANALYSIS

A. *Legal Standards*

1. Anticipation

Anticipation is a question of fact, as is the question of what a prior art reference teaches. *In re NTP, Inc.*, 654 F.3d 1279, 1297 (Fed. Cir. 2011). "A claim is anticipated only if each and every element as set forth in the

[2] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102, 103. Because the '121 patent has an effective filing date before the effective date of the applicable AIA amendment, we refer to the pre-AIA version of §§ 102 and 103.
[3] U.S. Patent No. 7,330,168 B2, issued Feb. 12, 2008, filed Apr. 30, 2003 (Ex. 1003, "Anzai").
[4] U.S. Patent No. 6,992,332 B2, issued Jan. 31, 2006, filed May 5, 2003 (Ex. 1004, "Yamazaki").

claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, "a single prior art reference must expressly or inherently disclose each claim limitation"). Moreover, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

Whether a reference anticipates is assessed from the perspective of an ordinarily skilled artisan. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) ("[T]he dispositive question regarding anticipation [i]s whether one skilled in the art would reasonably understand or infer from the [prior art reference's] teaching that every claim element was disclosed in that single reference." (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991)). Additionally, under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates. *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002)

2. Obviousness

A claim is unpatentable under 35 U.S.C. § 103 if "the differences between the subject matter sought to be patented and the prior art are such

that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In conducting an obviousness analysis, one must determine whether the claimed elements are present in the prior art. *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1194–98 (Fed. Cir. 2014) (citing *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1164 (Fed. Cir. 2006)). However, a patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016); *see KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'").

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)); *see also Intelligent Bio-Sys.*, 821 F.3d at 1369. Therefore, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable.

B. *Level of Ordinary Skill in the Art*

The person of ordinary skill in the art is a hypothetical person who is presumed to know the relevant prior art. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey–Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)). In determining the skill level, the Board may consider various factors including "the type of problems encountered in the prior art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *Id.* In a given case, every factor may not be present, and one or more factors may predominate. *Id.*

Petitioner describes a person of ordinary skill in the art ("POSITA" or "ordinarily skilled artisan") at the time of the invention as having "a Bachelors' degree in electrical engineering or a comparable field of study, plus approximately two to three years of professional experience with electronic and optoelectronic device design" and notes that "[a]dditional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education." Pet. 5–6 (citing Ex. 1002, Neikirk Decl., ¶ 23).

Patent Owner's expert, Dr. Bretschneider testifies that

> In my opinion, the field of "electronic and optoelectronic device design" is too broad. A POSITA of the '121, had at least a Bachelors' degree in a field of engineering or physics and at least two to three years of professional experience related to the design and manufacture of the relevant aspects of flat panel displays. Additional relevant graduate education related [sic] could reduce but not eliminate the time requirement for professional experience. While Dr. Neikirk proposes a different definition of a POSITA, the differences do not have material effect on my opinions rendered below. Regardless of which definition of a POSITA were used, my conclusions would remain the same

Ex. 2005, Bretschneider Decl., ¶ 39.

We agree with and will apply Petitioner's statement of the level of ordinary skill in the art. This level of ordinary skill is reflective of the education and experience that would have been required to understand the problems and solutions identified in the '121 patent and the prior art. *Okajima v. Bourdeau*, 261 F.3d 1350 (Fed. Cir. 2001). We note that our conclusions would be the same even if we applied Patent Owner's slightly narrower definition of a POSITA.

C. *Claim Construction*

In an *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). This standard includes "construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). "Any prior claim construction determination concerning a term of the claim in a civil action,

or a proceeding before the International Trade Commission, that is timely made of record in the *inter partes* review proceeding will be considered." *Id.*

"In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek*, Inc., 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317.

"The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

In the preliminary phase of this proceeding, neither party sought construction of any term. *See* Inst. Dec. 8. In its Patent Owner Response, Patent Owner proposed constructions for two terms found in dependent claim 3. Claim 3 depends from claim 1, and further recites "where in the second dielectric layer comprises a passivation layer and a capping layer." Ex. 1001, 8:57–58. Patent Owner seeks construction of the terms "passivation layer" and "capping layer." PO Resp. 6–8. We consider each in turn.

1. "Passivation Layer"

In its Patent Owner Response, Patent Owner argues that "passivation layer" has a plain and ordinary meaning in the art. PO Resp. 7. Namely,

that "[a] passivation layer is a layer of a material that renders the surface layer below chemically passive or unreactive, especially by tying up dangling bonds." *Id.* (citing Ex. 2005, Bretschneider Decl., ¶ 66; Ex. 2010, 63; Ex. 2011, 256–57). Patent Owner asserts that "[a] dangling bond is an electron on the surface of a semiconductor crystal that lacks a neighboring atom to bond with, which creates an electrically active surface state that negatively impacts the performance of the semiconductor." *Id.* (citing Ex. 2005, Bretschneider Decl., ¶ 66; Ex. 2008, 7). Patent Owner contends that "[d]angling bonds are passivated with an inorganic dielectric layer (such as silicon nitride or silicon dioxide) that is designed to chemically and electrically stabilize the semiconductor surface by neutralizing dangling bonds." *Id.* (citing Ex. 2005, Bretschneider Decl., ¶ 66; Ex. 2008, 9). Patent Owner asserts that this is consistent with the '121 Patent's disclosure of a "passivation silicon nitride" layer. *Id.* (citing Ex. 1001, 5:34–36). Patent Owner notes that "[p]assivation is a distinct word from 'insulation' and 'planarization.'" *Id.* (citing Ex. 2011, 265–66). Thus, Patent Owner argues "a passivation layer is not the same as an "insulator" (a layer that electrically insulates) and is not the same as a 'planarization layer' (a layer that makes a flat, planar surface on top)." *Id.* at 8.

Petitioner argues that Patent Owner's construction, which requires tying up dangling bonds, is incorrect. Pet. Reply 1–5. Petitioner notes that there is no support in the Specification for this construction. *Id.* at 2. In particular, Petitioner notes that Patent Owner argues that tying up chemical bonds is necessary to improve semiconductor performance, but the passivation layer in the '121 patent embodiments is formed over metal, not semiconductor layers. *Id.* at 1 n.1 (citing Ex. 1001, 5:34–36, Fig. 2).

Petitioner also identifies a number of dictionary definitions, which suggest a broader construction. *See id.* at 2–4 (citing Ex. 1012, 140; Ex. 1013, 542; Ex. 1014, 798). Petitioner argues that these dictionaries confirm that the plain and ordinary meaning of passivation layer encompasses a layer that serves a physical barrier, with no consideration that the underlying layer be rendered chemically passive or unreactive by tying up dangling bonds. *Id.* at 3 (citing Ex. 1020, Neikirk Reply Decl., ¶ 10). Petitioner points to a number of prior art patents, which were originally assigned to the same assignee as the '121 patent—Au Optronics Corp.—that use organic materials for passivation layers. *See id.* at 11–13 (citing Ex. 1016, 2:47–52; Ex. 1018 ¶ 22; Ex. 1019 ¶ 30).

In its Sur-reply, Patent Owner argues that Petitioner's contention that "passivation" only requires "insulation" is too broad. PO Sur-reply 2–8. Patent Owner notes that the '121 patent distinguishes between "dielectric layers" and the "passivation" and "capping" layers, which indicates that they have different meanings. *Id.* at 2–3. Patent Owner argues that the Specification indicates that the "passivation" and "capping" layers are not merely planarization layers because they are not flat. *Id.* at 3–4. As for the extrinsic evidence, Patent Owner asserts that the definitions "consistently define 'passivation' in terms of its unique function: rendering the underlying surface stable." *Id.* at 4. Patent Owner submits that "[a] passivation layer is not just an insulating material—it also renders the surface of the layer below chemically passive or unreactive." *Id.* Patent Owner contends that it does not matter if we adopt Dr. Bretschneider's exact construction, because Petitioner has failed to meet any of the dictionary definitions that have been proffered. *Id.* at 7–8.

We begin with the language of the claims. *See Phillips*, 415 F.3d at 1314. As reproduced above, claim 3 recites that the "passivation layer" and "capping layer" are components of the "second dielectric layer." Claim 1 recites that the "second dielectric layer" is a component of the "second capacitor" and "over the second conductive layer." Claim 1 further recites that the "third conductive layer" is "over the second dielectric layer." We agree with Patent Owner that this claim language indicates that "passivation layer" is narrower than simply a "dielectric layer," but the claim language otherwise neither supports nor undermines the remainder of Patent Owner's construction.

We turn next to the Specification. "The specification is the 'single best guide to the meaning of a disputed term,' . . . and 'is, thus, the primary basis for construing the claims.'" *Trs. of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1362 (Fed. Cir. 2016) (citations omitted). As Petitioner notes, there is no definition in the Specification or any discussion of functions that Patent Owner now seeks to read into the limitation. Indeed, Patent Owner's sole citation to the '121 patent is the statement: "A layer of passivation silicon nitride (SiN) 212 is formed over ILD 208 and second metal patterns 210A and 210B." *See* PO Resp. 7 (citing Ex. 1001, 5:34–36). However, we agree with Petitioner that this sentence does not suggest that passivation layer 212 renders surfaces of ILD 208 or second metal patterns 210A/210B on which it is formed chemically passive or unreactive, let alone by tying up dangling bonds. Pet. Reply 2. Moreover, we note that Patent Owner's justification for the "tying up dangling bonds" requirement is that a dangling bond "negatively impacts the performance of the semiconductor," but in the disclosed embodiment of the

'121 patent, the passivation layer is formed over the dielectric and the metal layers, not the semiconductor. *See* Ex. 1001, 5:34–36. As for Patent Owner's contention that the disclosed embodiment shows the passivation layer as not flat, we do not agree that supports its construction. The fact that the passivation layer need not be flat does not mean that it necessarily is not flat, like the layer in Anzai. Thus, overall the Specification does not support Patent Owner's requirement that the passivation layer must function by "tying up dangling bonds."

Finally, we consider the extrinsic evidence. We note that "while extrinsic evidence 'can shed useful light on the relevant art,' . . . it is 'less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317. In particular, we "may rely on dictionary definitions, 'so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents.'" *Trs. of Columbia Univ.*, 811 F.3d at 1363. Here, the dictionaries support a slightly broader construction than that offered by Patent Owner, but also supports other parts of Patent Owner's construction. The definitions offered are as follows:

> Passivation: (1) The application of an insulating layer of glass, SiO2, or nitride over circuits and circuit elements for protection against moisture, contaminants, or other harmful conditions. (2) The growth of an oxide or nitride layer on the surface of a semiconductor to provide electrical stability by isolating the surface from electrical and chemical conditions in the environment."

Ex. 1012, 140.

> Passivation: 1. The growth of an oxide layer on the surface of a semiconductor to provide electrical stability by protecting the surface against moisture, contamination, particles, and

> mechanical damage. This reduce reverse current leakage, increase breakdown voltages, and raises the power dissipation rating. . . . 3. A coating of an electrically inert material, such as glass or silicon dioxide, used to protect semiconductors or resistors from environmental contamination. . . . 4. The growth of an oxide layer on the surface of a semiconductor to provide mechanical protection by isolating the transistor surface from electrical, mechanical (scratching of metal), and chemical conditions in the environment. 5. The technique of providing a semiconductor device chip with an isolating layer or "skin" that protects it from contamination by unwanted impurity atoms or molecules. . .7. The formation of an insulating layer directly over a circuit or circuit element to protect the surface from contamination, moisture, or particles.

Ex. 1013, 542.

> Passivation: The process or process (physical or chemical) by means of which a metal becomes passive.

Ex. 1014, 798.

Patent Owner also offers one dictionary definition:

> Passivation: The protection of junctions, regions, layers, or surfaces of semiconductors by depositing a material which renders them chemically passive or unreactive. Used for instance to protect oxidation, contamination, and other perils of harsh environments. Two common techniques are glassification and oxide passivation.

Ex. 2010, 3.

Patent Owner also cites to the Wikipedia entry, which notes in the context of semiconductor device fabrication that "surface passivation refers not only to reducing the chemical reactivity of the surface but also to eliminating the dangling bonds and other defects that form electronic surface states, which impair performance of the devices." Ex. 2013, 1. We note that same entry also states that "passivation is coating a material so that it

becomes 'passive', that is, less readily affected or corroded by the environment." *Id.*

We find these definitions to be of some help in construing this term. We find that the common thread is that a "passivation layer" is an insulating layer that provides protection from the environment to the layers below it. *See* Ex. 1012, 140; Ex. 1013, 542, Ex. 1014, 798; Ex. 2010, 3; Ex. 2013, 1. We find this construction to be most consistent with the broad claim language and the disclosure in the Specification. Although "tying up dangling bonds," may be a mechanism by which some materials provide such protection, nothing in the Specification or the extrinsic evidence provided appears to require that. Also, while chemical protection may be one kind of protection none of the evidence suggests that is the only protection that is provided. Moreover, nothing in the Specification supports reading a chemical protection requirement into the construction. Thus, we decline to adopt that portion of Patent Owner's construction. Instead, we construe passivation layer as "an insulating layer that provides protection from the environment to the layers below it."

We need not construe the term any further to resolve the parties' dispute over this claim language. *See Realtime*, 912 F.3d at 1375.

2. "Capping Layer"

Patent Owner argues that a "capping layer" is "a layer of hard material to protect a layer underneath, like how a hard 'cap' can be worn to protect the head." PO Resp. 8 (citing Ex. 2005, Bretschneider Decl., ¶ 67). Patent Owner asserts that "[t]his is consistent with the '121 Patent's disclosure of silicon nitride ('SiN') as the capping layer, as SiN is a hard, durable material." *Id.* (citing Ex. 2005, Bretschneider Decl., ¶ 67; Ex. 1001, 5:40–

42). Patent Owner contends that Petitioner's expert acknowledged that "capping" is distinct from the word "planarization." *Id.* (citing Ex. 2007, 51:18–52:4).

Petitioner disagrees with Patent Owner's construction. Pet. Reply 5–8. Petitioner responds that a POSITA would understand that the '121 patent does not ascribe any special meaning to "capping layer" other than it is an insulation material. *Id.* at 5. Petitioner argues that "[a]t most, a POSITA would understand capping layer to be an insulation layer covering (i.e., capping) an underlying layer or structure." *Id.* at 6. Petitioner submits that "[a] capping layer is not limited to providing a hard material," and "a POSITA would not associate a capping layer to be the uppermost layer in a layer stack, given that multiple layers (i.e., layers 218 and 220) are formed over capping layer 216 in the [']121 patent." *Id.* (citing Ex. 1001, Fig. 2; Ex. 1020, Neikirk Reply Decl., ¶ 13).

In its Sur-Reply, Patent Owner contends that "[i]f a 'capping layer' were simply an insulating layer, then claim 3 of the '121 Patent, which narrows the claimed dielectric layer to including both a capping layer and a passivation layer, would not be needed to specify both 'capping' and 'passivation' layers using distinct, different words," and "[d]ependent claim 3 does not merely call for additional 'insulation' layers." PO Sur-Reply 8. Patent Owner argues that the Specification supports its construction because the exemplary embodiment uses SiN as the capping layer, which is a hard material. *Id.* at 9. Patent Owner asserts that, regardless of whether the "capping layer" must be "hard," Petitioner has failed to show that any prior art teaches a capping layer that meets the other half of its definition, i.e., that the "capping layer" protects the layers underneath. *Id.* Finally, Patent

Owner submits that its construction is not indefinite, as Petitioner contends. *Id.* at 9–10. Patent Owner argues that a POSITA would have understood what materials are "reasonably durable" and "capable of protection" based on the context of the surrounding semiconductor layers. *Id.* at 10.

We begin with the language of the claims. As reproduced above, claim 3 recites that the "passivation layer" and "capping layer" are components of the "second dielectric layer." Claim 1 recites that the "second dielectric layer" is a component of the "second capacitor" and "over the second conductive layer." Claim 1 further recites that the "third conductive layer" is "over the second dielectric layer." Claim 4 depends from claim 3 and recites that "at least one of the passivation layer and the capping layer comprises silicon nitride." Nothing in this claim language supports Patent Owner's requirement that the "capping layer" be a "hard" material. Indeed, claim 4 suggests that the "capping layer" may be the same material, SiN, as the "passivation layer" or an entirely different material.

The Specification provides little insight into the meaning of "capping layer." In its description of Figure 2, the Specification states:

> A layer of capping SiN 216 is deposited to cover passivation SiN 212 and ITO pattern 214C. A layer of organics 218 is deposited over all of areas A, B, and C. Over area A, capping SiN 216 is also patterned to expose a portion of passivation SiN 212. Thus, organic **218** is also formed on passivation SiN 212 over area A. A layer of third metal 220 is formed over organic 218.

Ex. 1001, 5:40–46. The insights provided by the Specification are that the "capping layer" does not need to be the uppermost layer in a layer stack, given that the Specification discloses that multiple layers (organic 218 and metal 220) can be formed over the capping layer, and that the "passivation

layer" and "capping layer" can be the same material. *See id*. We do not see any support in the Specification for Patent Owner's requirement that the "capping layer" must be a "hard" material.

The parties offer testimony of their experts. *See* Ex. 2005, Bretschneider Decl., ¶ 69; Ex. 1020, Neikirk Reply Decl., ¶¶ 13–18. However, we do not find the testimony to be particularly illuminating on this dispute. Patent Owner's expert merely repeats Patent Owner's reasoning reproduced above. Petitioner's expert notes that the Specification does not support Patent Owner's construction. *See* Ex. 1020, Neikirk Reply Decl., ¶¶ 15–16.

We agree with Petitioner that there is no support in the intrinsic evidence for Patent Owner's requirement that the "capping layer" be a "hard" material. We also agree with Patent Owner that the "capping layer" must be more than just an insulation layer, because that does not give meaning to the word "capping." Instead, we find that Petitioner's alternative construction that a "capping layer" is an "insulation layer covering (i.e., capping) an underlying layer or structure" to be most consistent with the disclosure of the '121 patent. Thus, we construe a "capping layer" as simply "an insulation layer covering (i.e., capping) an underlying layer or structure."

We need not construe the term any further to resolve the parties' dispute over this claim language. *See Realtime*, 912 F.3d at 1375.

D. *Anticipation of Claims 1–3 and 5 by Anzai*

Petitioner contends that claims 1–3, and 5 are anticipated by Anzai. Pet. 7–21; Pet. Reply 9–15. Patent Owner disputes that the challenged claims are anticipated. PO Resp. 8–12; PO Sur-Reply 10–15.

1. Anzai (Ex. 1003)

Anzai relates to an EL display device "with a storage capacitance element for holding a video signal supplied to a gate of a driving transistor." Ex. 1003, 1:7–9. Each pixel portion includes a transistor that drives an EL element and a pixel selecting transistor that supplies a signal from the drain signal line to the gate of the driving transistor. *Id.* at 2:37–42. A storage capacitance element holds the signal supplied to the gate of the driving transistor. *Id.* at 2:37–45. The storage capacitance element includes an extension of the source of the pixel selecting transistor as a first capacitance electrode layer; a second capacitance electrode layer is disposed above the extension of the source, and a third capacitance electrode layer is connected to the source and disposed above the second capacitance electrode layer. *Id.* at 2:45–50.

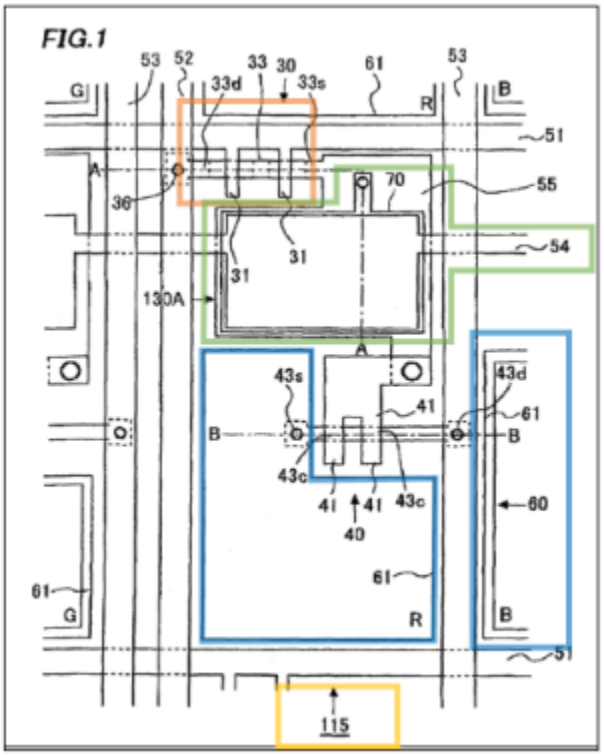
2. Analysis

a) Claim 1

(1) Limitation [1.pre]. [1.a], and [1.b]

As designated by Petitioner, the preamble of claim 1 [1.pre] recites "[a]n electroluminescence (EL device)," and limitation [1.a] recites "a substrate." Pet. vi. Petitioner notes that Anzai is directed to an EL display device having a reduced area for forming a storage capacitor that holds the video signal supplied to a transistor to improve the quality of the EL device display by holding the video supplied to the gate of a transistor that drives an OLED. *Id.* at 7 (citing Ex. 1003, code (57), 1:6–17). Petitioner cites Anzai as disclosing a substrate (limitation [1.a]) made of glass, synthetic resin, a conductive material, or a semiconductor. *Id.* at 7–8 (citing Ex. 1003, 3:57–61; Figs. 2A, 2B, 3A, 3B). As designated by Petitioner, limitation [1.b]

recites "a plurality of pixels formed on the substrate, each pixel being in a respective pixel area, each pixel area including at least a first area, a second area, and a third area." *Id.* at vi. Petitioner's annotated version of Figure 1 of Anzai is reproduced below (*Id.* at 9).



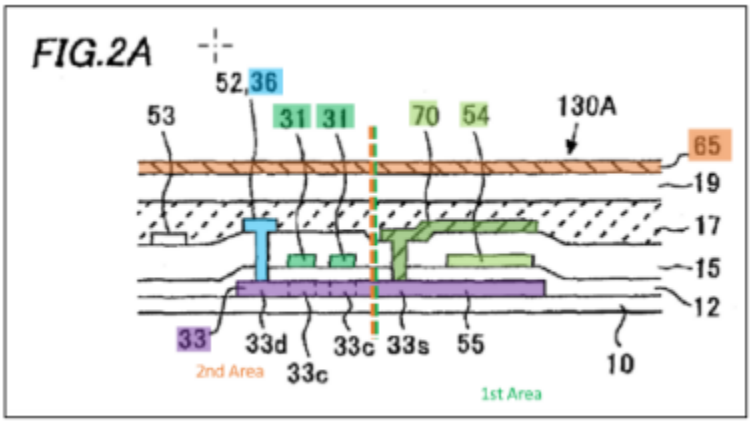
Petitioner's annotated version of Figure 1 of Anzai.

Patent Owner does not dispute that Anzai discloses these limitations. We have reviewed Petitioner's evidence and arguments and agree that Anzai discloses these limitations.

(2) Limitation [1.c]

As designated by Petitioner, claim limitation [1.c] recites "at least a first capacitor and a second capacitor in the first area, the first capacitor including a first conductive layer formed over a first gate oxide layer, a first dielectric layer over the first conductive layer, and a second conductive layer

over the first dielectric layer, and the second capacitor including the second conductive layer, a second dielectric layer over the second conductive layer, and a third conductive layer over the second dielectric layer." Pet. vi. Petitioner's annotated version of an embodiment of a pixel portion of an organic EL display device in Figure 2A of Anzai is reproduced below.



Pet. 10; *see also* Ex. 1003, 3:21–24. In this embodiment, Petitioner identifies a first capacitor in the first area as formed by electrode layers 54 and 70 with insulating film 15 sandwiched between them. Pet. 10. Petitioner notes that in Anzai, electrode layer 54 is formed over gate insulating film 12 formed of SiO_2 (an oxide layer). *Id.* (citing Ex. 1003, 3:61–67, 4:25–47, Fig. 2A; Ex. 1002, Neikirk Decl., ¶ 45). Petitioner identifies a second capacitor as formed between third electrode capacitance layer 70 and cathode layer 65, with an insulating layer comprising first and second planarization films 17 and 19 that function as a capacitance insulating film. *Id.* at 11 (citing Ex. 1003, 4:30–51, 5:58–67). Petitioner cites Dr. Neikirk's testimony that a person of ordinary skill in the art would have recognized the first and second capacitors share a second conductive layer, as recited in claim 1, because electrode layer 70 is common to both capacitors. *Id.* at 11–12 (citing Ex. 1002, Neikirk Decl., ¶ 47). Petitioner

also cites the embodiment in Anzai's Figures 3A and 3B as disclosing the same structure as that shown in Figure 2A, except for the addition of electrode layer 71 to the capacitance structure such that electrode layers 70 and 71 form a U-shaped structure conductive layer that is shared between the first and second capacitor. *Id.* at 12–13 (citing Ex. 1002, Neikirk Decl., ¶ 48; Ex. 1003, 5:52–61, 5:67–6:3). Thus, according to Petitioner, the claimed second capacitor is formed by the combined electrode layer 70/71 and cathode layer 65. *Id.*

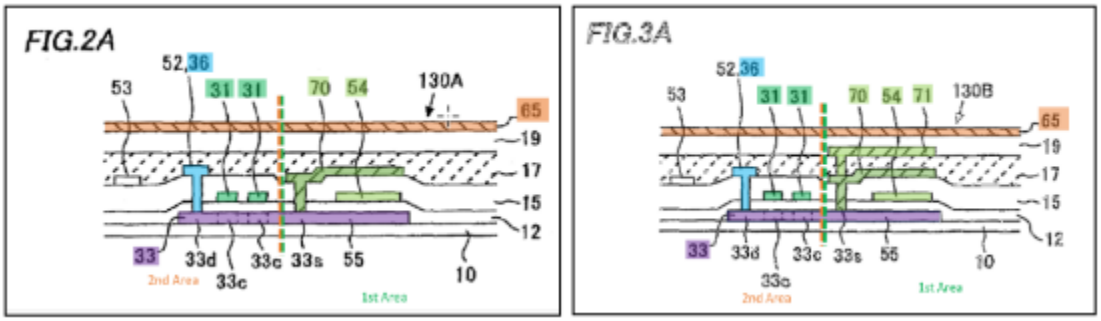
Patent Owner does not dispute that Anzai discloses this limitation. We have reviewed Petitioner's evidence and arguments and agree that Anzai discloses this limitation.

(3) Limitation [1.d]

As designated by Petitioner, claim limitation [1.d] recites

> a transistor in the second area, the transistor including a first semiconductor layer formed on the substrate, the first gate oxide layer over the first semiconductor layer, and a fourth conductive layer over the first gate oxide layer, wherein the fourth conductive layer is formed of the same conductive film as the first conductive layer, and wherein both the first conductive layer and the fourth conductive layer are directly formed on the gate oxide layer.

Pet. vi. Petitioner identifies Anzai's pixel selecting transistor 30 as corresponding to the transistor recited in claim 1. *Id.* at 13–14. Petitioner's annotated version of embodiments of pixel portions of an EL display device shown Figures 2A and 3A of Anzai is reproduced below.



Id. at 15; *see also* Ex. 1003, 3:6–12. Petitioner states that transistor 30 is formed in the transistor area discussed above by gate electrode 31 above active layer 33 with gate insulating film 12 between them; drain electrode 36 is connected to drain 33d and third capacitance electrode layer 70 is connected to source 33s. Pet. 15 (citing Ex. 1003, 4:1–25, 4:37–40, Figs. 2A, 3A; Ex. 1002, Neikirk Decl., ¶¶ 50–53). Petitioner notes that the device is fabricated using sequentially deposited layers by (i) depositing an amorphous silicon film on substrate 10 and recrystallizing it to form a polycrystalline film that functions as active layer 33 (the claimed first layer), (ii) forming a single or multiple layers of SiO_2 and SiN on layer 33 to serve as gate insulating film 12 (the claimed fourth layer), and (iii) disposing on gate insulting film 12 gate signal line 51 that works as gate electrode 31. *Id.* at 14 (citing Ex. 1003, 4:11–14, Figs, 2A, 3A; Ex. 1002, Neikirk Decl., ¶ 52).

According to Petitioner, Anzai's gate electrode 31 (the claimed fourth conductive layer) is formed of the same conductive film as first electrode layer 54 (the claimed first conductive layer) because Anzai discloses each as being formed directly on the gate insulating layer 12 (the same underlying structure) by the same process and of the same material. *Id.* at 15 (citing Ex. 1003, 4:25–40 (stating that second capacitance electrode layer 54 is

made of Cr or Mo and formed in the same layer as gate electrode 31 by the same process), Figs. 2A, 3A). Petitioner asserts that an ordinarily skilled artisan would have understood that forming electrode layers in the same layer by the same process with the same material would mean that the two electrode layers are formed of the same conductive film. *Id.* (citing Ex. 1002, Neikirk Decl., ¶ 53).

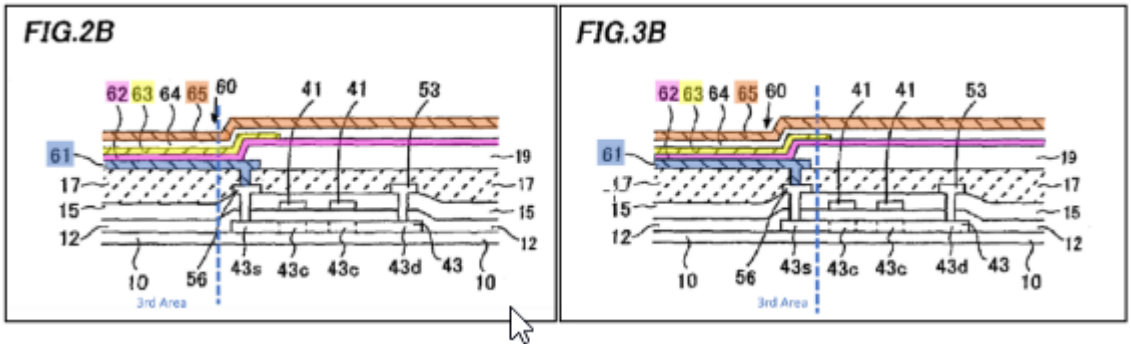
Patent Owner does not dispute that Anzai discloses this limitation. We have reviewed Petitioner's evidence and arguments and agree that Anzai discloses this limitation.

(4) Limitation [1.e]

As designated by Petitioner, claim limitation [1.e] recites

> a light emitting device in the third area, the light emitting device including a fifth conductive layer, a first organic layer over the fifth conductive layer, and a sixth conductive layer over the first organic layer, wherein the sixth conductive layer is formed of the same conductive film as the third conductive layer.

Pet. vi. Petitioner's annotated version of the pixel embodiments shown in Figure 2B and 3B of Anzai is reproduced below.



Pet. 16. Petitioner cites Anzai as disclosing a third OLED area with anode layer 61 (the claimed fifth conductive layer) connected to active source 43a through electrode 56, emissive layer 63 (the claimed first organic layer) over

anode layer 61 (the claimed fifth conductive layer), and cathode layer 65 (the claimed sixth conductive layer) over emissive layer 63 (the claimed first organic layer) formed of the same conductive film as cathode layer 65 (the claimed third conductive layer). *Id.* at 15–16 (citing Ex. 1002, Neikirk Decl., ¶¶ 54–57; Ex. 1003, 5:3–33, Figs. 2B, 3B). Petitioner notes that EL element 60 includes anode layer 61 made of the transportation electrode, e.g., Indium Tin Oxide, hole transportation layer 62, emissive layer 63, electron transportation layer 64, and cathode layer 65. *Id.* at 16–17. According to Petitioner, an ordinarily skilled artisan would have understood (i) that emissive layer 63 is organic because organic molecules are activated during operation, (ii) that intervening layers 62, 64 in organic element 60 do not change the relative positions of the layers recited in claim 1, because emissive layer 63 is over anode 61 and cathode layer 65 is over emissive layer 63, and (iii) that cathode layer 65 (the claimed sixth conductive layer) is formed from the same conductive film as the third conductive layer of the second capacitor because the same film that serves as the third conductive layer serves as the sixth conductive layer. *Id.* at 17 (citing Ex. 1002, Neikirk Decl., ¶¶ 56–57).

Patent Owner does not dispute that Anzai discloses this limitation. *See* PO Resp. We have reviewed Petitioner's evidence and arguments and agree that Anzai discloses this limitation.

(5) Summary

We find that Petitioner has shown by a preponderance of the evidence that Anzai discloses all the limitations of claim 1 as arranged in that claim. Accordingly, we find that Petitioner has shown by a preponderance of the evidence that Anzai anticipates claim 1.

b) Claims 2 and 5

Petitioner also maps the disclosure of Anzai to dependent claims 2 and 5. Pet. 18–19, 21. Patent Owner does not dispute that Anzai discloses the limitations of these claims. We have reviewed Petitioner's evidence and contentions and find that Petitioner has shown by a preponderance of the evidence that claims 2 and 5 are anticipated by Anzai.

c) Claim 3

Claim 3 depends from claim 1 and recites "the second dielectric layer comprises a passivation layer and a capping layer." Petitioner notes that the '121 patent describes a passivation layer 212 of SiN formed over ILD208 and second metal patterns 210A and 210B and a SiN capping layer 216 disposed to cover passivation layer 212 and ITO pattern 214C. Pet. 19 (citing Ex. 1001, 5:34–36, 5:40–42). Petitioner also asserts that, other than describing them as separate layers, the '121 patent does not ascribe any special meaning to the terms passivation layer and capping layer. *Id.* (citing Ex. 1002, Neikirk Decl., ¶ 61). According to Petitioner, consistent with the '121 patent description, an ordinarily skilled artisan would have understood that the passivation and capping layer need not be made of different materials. *Id.* (citing Ex. 1002, Neikirk Decl., ¶ 61).

Petitioner notes that Anzai's first planarization film 17 and second planarization film 19 function as the capacitance insulating film in the first embodiment, and that, although Anzai does not specify the material for planarization layer 19, it is the sole layer between electrode layer 71 and cathode layer 65 forming the second capacitor. *Id.* at 19–20. Petitioner contends that an ordinarily skilled artisan would have understood that when first and second planarization layers 17 and 19 are used as the insulating

films, one of the layers can be understood as a passivation layer and the other layer as a capping layer, as claimed.[5] *Id.* at 19–20.

Patent Owner argues that Anzai's planarization layers cannot be a "passivation layer" and a "capping layer." PO Resp. 8–12. Relying on its definition for "passivation layer," Patent Owner argues that Anzai's planarization layer does not passivate. *Id.* at 9–11. In particular, Patent Owner argues that "Anzai's planarization film 17 cannot also be a passivation layer because it is made of organic resin, which is not a suitable material for passivation." *Id.* at 11 (citing Ex. 2005, Bretschneider Decl., ¶¶ 69–73). Patent Owner asserts that organic resins cannot passivate. PO Sur-reply 11 (citing Ex. 1015, 48:20–49:5).

Patent Owner also argues that Anzai's "second planarization film 19" cannot be the claimed "capping layer." PO Resp. 12. Patent Owner submits that "[a]s admitted by Petitioner, 'Anzai does not disclose the material for planarization layer 19.'" *Id.* (quoting Pet. 20). Patent Owner asserts that that "a capping layer is a hard material intended to protect components underneath—such as the silicon nitride layer described by the '121 Patent." *Id.* (citing Ex. 2005, Bretschneider Decl., ¶ 74; Ex. 1001, 2:31–33, 5:40–44). Patent Owner contends that "[b]ecause Petitioner admits that Anzai does not disclose the material of planarization layer 19, Petitioner cannot show that Anzai's planarization layer 19 is strong or hard enough to protect layers underneath." *Id.* Patent Owner argues that "Anzai does not describe

[5] Petitioner submitted a supplemental brief on allegedly inconsistent positions taken by Patent Owner in the underlying district court litigation on this issue. *See* Pet. Supp. Br.; PO Supp. Resp. However, because we have not adopted Patent Owner's constructions of these terms, we do not need to address this supplemental briefing.

planarization film 19 as performing any such role, and there is no reason a POSITA would understand that planarizing film 19 is a capping layer." *Id.* Patent Owner asserts that "the disclosure of Anzai simply supports that planarizing film 19 is just a layer that provides a flattened topography—it does not describe using a material suitable for capping." *Id.*

As we explained above, we disagree with Patent Owner's narrow constructions for "passivation layer" and "capping layer." We find that Petitioner has presented sufficient evidence to show that Anzai discloses both a "passivation layer" and a "capping layer."

As we explained above, we have construed "passivation layer" to mean "an insulating layer that provides protection from the environment to the layers below it." Petitioner has shown that "first planarization film 17" is an insulating layer. *See* Ex. 1002 ¶¶ 62–65. We further find that Petitioner has shown sufficiently that "first planarization film 17" is "formed over the entire surface for flattening, which will protect the semiconductor surface from the surrounding environment." *Id.* ¶ 63. We have rejected Patent Owner's contentions that the film must tie up "dangling bonds," and instead determined that protecting the surface from the environment is sufficient. Thus, we find that Petitioner has shown by a preponderance of the evidence that Anzai discloses the "passivation layer" of claim 3.

As we explained above, we have construed "capping layer" to be "an insulation layer covering (i.e., capping) an underlying layer or structure." Here, Petitioner has shown that Anzai's planarization film 19 meets the claimed "capping layer." *See* Pet. 20. We find that Petitioner has shown that it is more likely than not that "planarization film 19" is made of insulating material. As Dr. Neikirk persuasively testifies,

> Anzai discloses that planarization layer 17 may be made of an organic resin for flattening the surface. EX1003, 4:20-24. While Anzai does not disclose the material for planarization layer 19, it must be made of an insulation material because in the embodiment of Fig. 3A, it is the sole layer between electrode layer 71 and cathode layer 65 forming the second capacitor. *Id.*, 6:3–8; Fig. 3A. Moreover, Anzai discloses that the first planarization film 17 and the second planarization film 19 for the first embodiment "function as the capacitance insulating film for this configuration." *Id.*, 5:62–67.

Ex. 1002, Neikirk Decl., ¶ 62. We find this testimony well-reasoned and entitled to substantial weight. We further agree with Dr. Neikirk that a "POSITA would further understand that the second planarization film 19 is then further disposed on the first planarization film 17 (capping the passivation layer)." *Id.* ¶ 63 (citing Ex. 1003, 5:3–13; Figs. 2A–B, 3A–B). Thus, we find that Petitioner has shown by a preponderance of the evidence that Anzai discloses the claimed "capping layer."

Accordingly, we find that Petitioner has shown by a preponderance of the evidence that claim 3 is anticipated by Anzai.

E. *Obviousness of Claim 4 Over Anzai and Yamazaki*

Petitioner argues that claim 4, which depends from claim 3, would have been obvious over the combination of Anzai and Yamazaki. Pet. 22–27. Patent Owner opposes. PO Resp. 13–18.

1. Yamazaki

Yamazaki concerns a light emitting device using a light emitting element having a layer that contains an organic compound between a pair of electrodes on which an electric field is applied to obtain fluorescence or phosphorescence. Ex. 1004, 1:7–12. Yamazaki's light emitting device has a pixel part that includes a plurality of light emitting elements between first

and second substrates, which have their respective insulating surfaces and a driving circuit including a plurality of thin film transistors; the light emitting element has a first electrode, a layer containing an organic compound in contact with the first electrode, and a second electrode in contact with a layer containing the organic compound. *Id.* at 2:42–51. Yamazaki discloses a number of manufacturing steps that seek to improve manufacturing yield and improve reliability. *See generally id*. at 2:42–7:67.

2. Claim 4

Claim 4 depends from claim 3 and recites "at least one of the passivation layer and the capping layer comprises silicon nitride." Petitioner cites Anzai as disclosing a second dielectric layer comprises a first passivation layer (first planarization layer 17) and a capping layer (second planarization layer 19). Pet. 23, 45; *see* Section III.D.2.c herein. Petitioner acknowledges that Anzai does not explicitly state what materials are used to form planarization layers 17 and 19 (other than organic resin for layer 17), but argues that Anzai discloses those layers function as the capacitance insulating film. Pet. 45 (citing Ex. 1003, 4:20–24, 5:62–6:9). Petitioner also argues Anzai teaches that SiN can be used as interlayer insulating film 15 between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitor element 130 and in gate insulating film 12 between first and second capacitance layers 55, 54. *Id.* at 23; *see also id.* at 45 (citing Ex. 1003, 4:8–10, 4:17–24, 4:40–47, 5:62–6:9).

Petitioner asserts that Yamazaki discloses the claimed passivation layer, i.e., insulating material 30 disposed between cathode 32 and electrodes 46, 47, 48, 24, and 23, in a manner similar to Anzai's layer 17 and 19, disposed between cathode 65 and electrodes 53, 52, 71, where the top

surface is flattened relative to the topology underneath, using, e.g., a chemical mechanical polish process. *Id.* at 24–25 (citing Ex. 1004, 20:17–24); *see also id.* at 42–43 (citing Ex. 1004, Fig. 2; Ex. 1002, Neikirk Decl., ¶¶ 110–121). Petitioner also cites Yamazaki as disclosing SiN is a suitable material for layer 30 and argues it would have been obvious to an ordinarily skilled artisan to use SiN for at least one of Anzai's planarization films 17 or 19. *Id.* at 23–27 (citing Ex. 1004, 11:45–50; Ex. 1002, Neikirk Decl., ¶ 76). Thus, according to Petitioner, an ordinarily skilled artisan would have had reason to modify Anzai to use inorganic materials, such as SiN, for Anzai's films 17 and 19. *Id.*

Patent Owner notes that claim 4 depends from claim 3, and contends that Petitioner's arguments suffer from the same defects it raised with respect to claim 3. PO Resp. 13. Patent Owner further responds that Petitioner has failed to show a motivation to combine Anzai with Yamazaki. *See id.* at 13–18. Patent Owner, supported by the testimony of Dr. Bretschneider, explains that "Anzai explicitly taught that planarization layer 17 is an organic resin—and a POSITA would have recognized that an organic resin is a perfectly suitable material for insulation in Anzai's configuration." *Id.* at 13 (citing Ex. 2005, Bretschneider Decl., ¶ 78; Ex. 1003, 4:23–24, 5:3–5). Thus, Patent Owner argues that a "POSTIA [sic] would have had no reason to deviate from Anzai's teaching (at least, not without hindsight)." *Id.*

Patent Owner asserts that "Anzai discloses using an 'SiN film' elsewhere in its structure (to 'form the interlayer insulating film') but specifically teaches using an organic resin material for planarization layer 17." *Id.* at 13–14 (citing Ex. 1003, 4:17–18, 4:23–24). Patent Owner argues

"a POSITA would have preferred an organic resin over silicon nitride for a planarization layer." *Id.* at 14 (citing Ex. 2005, Bretschneider Decl., ¶ 79). Patent Owner contends that "[t]his is because organic resins flow more easily to fill out dips in the surface below, whereas silicon nitride is usually deposited via chemical vapor deposition or sputtering and requires additional steps (like chemical mechanical polishing) to make flat." *Id.* (citing Ex. 2005, Bretschneider Decl., ¶ 79; Ex. 1004, 11:34–37). Patent Owner submits that "[o]rganic resins are also softer than silicon nitride, so organic resins are less likely to crack or delaminate," and "[o]rganic resins can be spin coated and cured at lower temperatures—a cheaper process than chemical vapor deposition of silicon nitride." *Id.*

Patent Owner submits that this "appears to have been Anzai's thinking," because Anzai uses SiN in interlayer insulating film 15 between second and third capacitance layers 57 and 70, and in gate insulating film 12, but teaches that "planarization film 17 [is] made of an organic resin for flatting the surface." *Id.* at 15 (citing Ex. 1003, 4:22–24). Patent Owner contends that "Anzai taught the use of silicon nitride for layers 15 and 12 that are not flat, and the use of an organic resin for layers that are flat—especially layer planarization film 17." *Id.*

As for Yamazaki, Patent Owner argues that Petitioner provides no justification for selecting silicon nitride from the range of choices listed in Yamazaki. *Id.* at 15–16 (citing Ex. 1004, 11:45–58). Patent Owner submits that "[t]his is particularly the case when Anzai explicitly teaches using an organic resin for its ***planarization*** layer (as opposed Yamazaki's 'insulating material,' which may or may not be planarized)." *Id.* at 16 (citing Ex. 1004, 11:22–33). Patent Owner also argues that Yamazaki's teaching "relates to **a**

single layer 30 and is not applicable to **both** layers 17 and 19 of Anzai." Patent Owner asserts that unless both the layers are SiN, they cannot meet its constructions for "passivation layer" and "capping layer." *Id.* at 17–18.

We find Petitioner has shown by a preponderance of the evidence that the combination of Anzai and Yamazaki teach the limitations of claim 4, and that there would have been a motivation to combine the references with a reasonable expectation of success. As we explained above, we do not adopt Patent Owner's constructions of "passivation layer" and "capping layer," so Patent Owner's arguments that the combination does not teach either a "passivation layer" or "capping layer" (depending on which layer is replaced with silicon nitride), PO Resp. 17–18, are not persuasive because it is founded on Patent Owner's claim construction. Thus, we focus our attention on Patent Owner's arguments regarding the motivation to combine.

We find that Petitioner has shown sufficiently that there is a motivation to combine Anzai and Yamazaki. *See* Pet. 25–27; Ex. 1002, Neikirk Decl., ¶¶ 78–79. First, Patent Owner argues that essentially silicon nitride is an inferior material to use for Anzai's planarization layer 17 compared with organic resin. PO Resp. 13–15. However, "[i]t's not necessary to show that a combination is the *best* option, only that it be a *suitable* option." *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 797, 800 (Fed. Cir. 2021) (emphasis in original).

Patent Owner does not argue that silicon nitride would not work, but rather that it would be more difficult and more expensive to use. *See* PO Resp. 14. But "the fact that the two disclosed apparatus[es] would not be combined by businessmen for economic reasons is not the same as saying that it could not be done because skilled persons in the art felt that there was

some technological incompatibility that prevented their combination. Only the latter is telling on the issue of nonobviousness." *Grit Energy Solutions LLC v. Oren Techs., LLC*, 957 F.3d 1309, 1323 (Fed. Cir. 2020) (quoting *Orthopedic Equip. Co., Inc. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983)). "Likewise, a given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine." *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006). Here, Petitioner explains that "a POSITA would have known that organic materials usually have lower dielectric constants than inorganic materials, such as SiN, and a higher dielectric constant is desirable for the insulator in a capacitor since that leads to higher capacitance per unit area." Pet. 26 (citing Ex. 1002, Neikirk Decl., ¶ 78). Petitioner further explains that this "then allows a reduced area storage capacitance element, one of the objectives of Anzai." *Id.* (citing Ex. 1003, code (57)). Patent Owner's focus mainly on planarization (PO Sur-reply 16–17) ignores that the Anzai's planarization layers 17 and 19 also "function as the capacitance insulating film." Ex. 1003, 5:65–67. Thus, although there are tradeoffs, Petitioner has shown sufficiently that a POSITA would have been motivated to incorporate the teachings of Yamazaki regarding potential materials for planarization layers 17 and 19.

Second, Patent Owner argues that a Petitioner has failed to provide an adequate reason to select silicon nitride from Yamazaki's list of potential materials. We disagree. Petitioner has explained the benefits of selecting a high dielectric inorganic material. Pet. 26. Yamazaki provides only three potential options—silicon oxide, silicon nitride, and silicon oxynitride. *See* Ex. 1004, 11:45–50. Moreover, Dr. Neikirk testified, supported by multiple

references, that using silicon nitride was well known in the prior art at the time of the invention. *See* Ex. 1002, Neikirk Decl., ¶ 75 (citing Ex. 1007; Ex. 1008; Ex. 1009). "When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421. Indeed, "[i]f a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability." *Id.* at 417. This is the case here. Petitioner has shown that a person of ordinary skill seeking to improve the capacitance of Anzai's planarization layers 17 and 19, without increasing the size of the capacitor, would have looked at the inorganic materials identified in Yamazaki as suitable for the purpose, and it would have been would obvious to choose silicon nitride, a well-known, and predictable material for the application. Thus, we disagree with Patent Owner that Petitioner has failed to show a sufficient reason for selecting silicon nitride from Yamazaki's list of suitable materials.

Third, Patent Owner argues that Petitioner's contentions only support changing a single layer, but does not provide a reason to change both layers. PO Resp. 16–17. However, claim 4 only requires that one of the layers be silicon nitride. *See* Ex. 1001, 8:60–61 ("wherein *at least one of* the passivation layer and the capping layer comprises silicon nitride" (emphasis added)). Thus, there was no need for Petitioner to provide a reason to change both layers.

Finally, in its Supplemental Briefing, Patent Owner argues that Petitioner was making contradictory arguments between the district court litigation and this proceeding. *See* PO Supp. Br. In particular, Patent Owner

asserts that in response to an interrogatory asking for potential non-infringing design-arounds, Petitioner contended that the layer identified by Patent Owner as the "capping layer" "serves no purpose . . . and could be omitted." *Id.* at 2 (citing Ex. 2014, 29–30, 32). Patent Owner argues that "[i]f such a silicon nitride capping layer would 'serve[] no purpose and could be omitted' according to Petitioner's interrogatory response, then a POSITA would not have been motivated to select or use it." *Id.* We do not agree with the contention that a Petitioner's statement that a particular layer in a completely different device "serves no purpose" and "could be omitted" is particularly probative of Anzai's device or proposed changes to Anzai. We find this given that Anzai identifies a purpose for these layers and states that "[b]oth the first planarization film 17 and the second planarization film 19 function as the capacitance insulating film in this configuration." Ex. 1003, 5:65–67. Thus, we disagree that Petitioner is necessarily making a contradictory statement or that it is probative of obviousness for this ground in this proceeding.

Accordingly, we find that Petitioner has shown by a preponderance of the evidence that the combination of Anzai and Yamazaki teaches all the limitation of claim 4, and that a person of ordinary skill would have been motivated to combine Anzai and Yamazaki in the manner proposed with a reasonable expectation of success. Thus, Petitioner has shown by a preponderance of the evidence that claim 4 would have been obvious over the combination of Anzai and Yamazaki.

F. *Obviousness of Claims 1–7 over Yamazaki and Anzai*

Petitioner argues that claims 1–7 would have been obvious over the combination of Yamazaki and Anzai. Pet. 27–52. Patent Owner opposes. PO Resp. 18–21.

1. Claim 1

a) Limitations [1.pre], [1.a], [1.b]

Petitioner cites Yamazaki as disclosing an EL device having a substrate 10 on which driving circuits and pixel parts are formed. Pet. 27–28. Petitioner also cites Yamazaki as disclosing pixel part 2 comprising a plurality of pixels within an active-matrix light emitting device. *Id.* at 29. Petitioner notes that each of Yamazaki's pixel parts includes "capacity" 41 in a Capacitor Area (the claimed first area), a current controlling TFT in a TFT Area (the claimed second area), and an EL element in an EL Area (the claimed third area). *Id.* (citing Ex. 1004, 2:37–64, 8:63–9:4, 9:47–64, 9:47–10:55, 11:22–12:13, 20:3–21:7, Figs 1A, 2; Ex. 1002, Neikirk Decl., ¶ 85).

Patent Owner does not dispute that Yamazaki discloses these limitations. *See* PO Resp. 18–21. We have reviewed Petitioner's evidence and argument and find that Petitioner has proven by a preponderance of the evidence that Yamazaki discloses these limitations.

b) Limitation [1.c]

Petitioner cites Yamazaki as disclosing first and second capacitors in the first area (capacity 41). Pet. 30. Petitioner's annotated version of Figure 2 of Yamazaki is reproduced below.

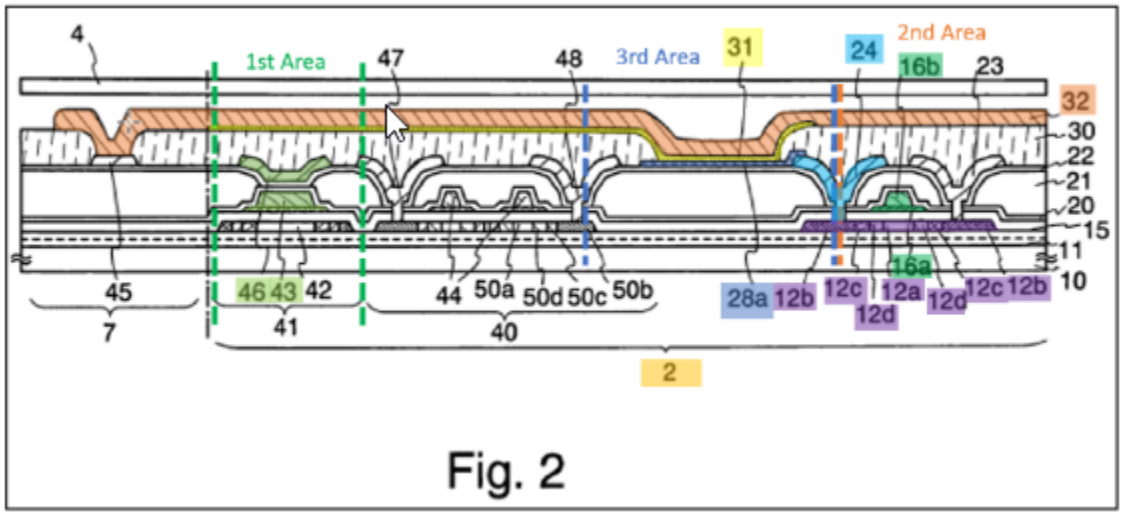


Fig. 2

Pet. 32. According to Petitioner, Yamazaki discloses a first capacitor in the first area formed by electrode 43 (the claimed first conductive layer) over gate insulating film 15 (the claimed first gate oxide layer), interlayer insultation films 20, 22 (the claimed first dielectric layer) over electrode 43 (the claimed first conductive layer), and electrode 46 (the claimed second conductive layer) over interlayer insulation films 20, 22 (the claimed first dielectric layer). *Id.* at 30–31. Petitioner asserts that, in the proposed combination, Yamazaki's second capacitor includes electrode 46 (the claimed second conductive layer), cathode 32, and sandwiched between them, insulating material 30 having a thickness selected according to the teachings of Anzai that acts as a dielectric material. *Id.* at 32 (citing Ex. 1004, 9:65–10:55, 11:22–12:13).

Petitioner acknowledges that Yamazaki does not disclose a capacitor formed between electrode 46 and cathode 32, but argues that, to an ordinarily skilled artisan, it would have been obvious to combine Yamazaki's teaching with those of Anzai for the formation of a storage capacitor using cathode 32, which extends from the third area into the first

area, as an electrode for a storage capacitor with electrode 46. Pet. 32–34 (citing Ex. 1002, Neikirk Decl., ¶ 89). In particular, Petitioner cites Anzai as disclosing a first capacitor between layers 54 and 55, a second capacitor between electrode layers 54 and 70 or 70/71, and a third capacitor between electrode layers 70 or 70/71 and cathode 65, which extends from the third area into the first area. *Id.* at 33 (citing Ex. 1003, 4:48–51; Ex. 1002, Neikirk Decl., ¶ 94).

According to Petitioner, applying Anzai's teaching of establishing a storage capacitor between electrode layer 70 and cathode layer 65 where first and second planarization layer 17 and 19 are the dielectric materials, a person of ordinary skill in the art would have understood that a capacitor can be formed between Yamazaki's electrode 46 and cathode 32, such that insulating material 30 and EL layer 31 act as the dielectric between the capacitor electrodes. *Id.* at 34 (citing Ex. 1002, Neikirk Decl., ¶ 97).

Patent Owner does not dispute that the combination of Yamazaki and Anzai teaches this limitation. *See* PO Resp. 18–21. To the extent that Patent Owner argues that there would not be a motivation to combine Yamazaki and Anzai, we have addressed those argument with respect to the combination of Anzai and Yamazaki above. We also note that those arguments do not address the specific combination proposed here where Petitioner starts with Yamazaki and adds certain features from Anzai. We have reviewed Petitioner's contentions and supporting evidence and find that Petitioner has shown sufficiently that the combination teaches this limitation and that Petitioner has shown a motivation to combine the reference with a reasonable expectation of success.

c) Limitation [1.d]

Referencing its annotated Figure 2, Petitioner cites Yamazaki as disclosing the claimed transistor in the second area in the form of an unnumbered current-controlling TFT arranged on pixel part 2 formed on substrate 10 below gate insulating film 15. Pet. 35–36 (citing Ex. 1004, 9:47–64, Fig. 2). Petitioner states that regions 12a–12d of the current controlling TFT (i.e., channel region 12a, high level impurity source and drain regions 12b, low impurity regions 12c, 12d over which gate electrode 16a, 16b are deposited) are a semiconductor layer, that gate insulating film 15 (constructed of a silicon oxide film) is formed over regions 12a–12d, and that gate electrode 16a/16b and electrode 43 are formed on gate insulating film 15. *Id.* at 35–36 (citing Ex. 1004, 10:31–33, Fig. 2; Ex. 1002, Neikirk Decl., ¶ 99).

Noting that Yamazaki does not explicitly disclose the materials used to form gate electrode 16a/16b and electrode 43, Petitioner observes that Yamazaki refers to gate electrode 16a/16b collectively as electrode 16 including first conductive layer 16a (a thin lower layer formed directly on insulation layer 15) and second conductive layer 16b (a narrower but thicker trapezoidal upper layer formed directly on lower layer 16a). *Id.* at 36 (citing Ex. 1004, 18:8–14, Fig. 2). Noting that electrode 43 has the same configuration (composition and general shape) as that of electrode 16, Petitioner contends it would have been obvious to an ordinarily skilled artisan to form electrode 16 and electrode 43 of the same conductive film. *Id.* at 36–37 (citing Ex. 1004, Fig. 2; Ex. 1002, Neikirk Decl., ¶ 101). Petitioner further states that, consistent with Yamazaki's disclosure and the common semiconductor manufacturing practice of forming multiple

components in the same processing steps (e.g., layer deposition and patterning), an ordinarily skilled artisan would have understood that Yamazaki discloses that terminal electrode 19a/19b in Figure 1B has the same configuration as electrode 43 in Figure 2 and would have formed them in the same step as an efficient manufacturing process. *Id.* at 37–39.

Patent Owner does not dispute that Yamazaki teaches this limitation. *See* PO Resp. 18–21. We have reviewed Petitioner's contentions and supporting evidence and find that Petitioner has shown sufficiently that Yamazaki teaches this limitation.

d) Limitation [1.e]

Petitioner cites Yamazaki as disclosing in the EL area a first electrode 28a that functions as an anode of the EL element formed on anode 28 (the claimed fifth conductive layer) and second electrode 32 (the claimed sixth conductive layer) that functions as the cathode also formed over EL layer 31 (the claimed first organic layer), such that cathode 32 (in the third area) is formed of the came conductive film as the third conductive layer. Pet. 39–41 (citing Ex. 1002, Neikirk Decl., ¶ 106). Petitioner also notes that anode layer 28a may be transparent conductive film, e.g., ITO, and cathode 32 is deposited on top of EL layer 31, which functions as wiring common to all pixels. *Id.* at 39–40 (citing Ex. 1002, Neikirk Decl., ¶ 104).

Patent Owner does not dispute that Yamazaki teaches this limitation. *See* PO Resp. 18–21. We have reviewed Petitioner's contentions and supporting evidence and find that Petitioner has shown sufficiently that Yamazaki teaches this limitation.

e) Summary

We find that Petitioner has shown by a preponderance of the evidence that the combination of Yamazaki and Anzai teaches all of the limitations of claim 1 and that a person of ordinary skill in the art would have been motivated to combine the references in the manner suggested with a reasonable expectation of success. Thus, we find that Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over the combination of Yamazaki and Anzai.

2. Claims 2, 5, and 6

Petitioner also maps the disclosures of Yamazaki and Anzai to dependent claims 2, 5, and 6. Pet. 41, 47–52. Patent Owner does not dispute that the combination of Yamazaki and Anzai teaches the limitations of these claims, and that a person of ordinary skill in the art would have been motivated to combine the references with a reasonable expectation of success. We have reviewed Petitioner's evidence and contentions and find that Petitioner has shown by a preponderance of the evidence that claims 2, 5, and 6 would have been obvious over the combination of Yamazaki and Anzai.

3. Claims 3 and 4

Petitioner notes that the '121 patent does not define the claimed passivation layer and capping layer that comprise the second dielectric layer. Pet. 42. Petitioner cites Anzai's disclosure of planarization layer 19 as the claimed capping layer. *Id.* (citing Ex. 1002, Neikirk Decl., ¶¶ 110–121). Petitioner asserts that Yamazaki discloses the claimed passivation layer, i.e., insulating material 30 disposed between cathode 32 and electrodes 46, 47, 48, 24, and 23, in a manner similar to Anzai's layers 17 and 19, disposed

between cathode 65 and electrodes 53, 52, 71, where the top surface is flattened relative to the topology underneath. *Id.* at 42–43 (citing Ex. 1004, Fig. 2; Ex. 1002, Neikirk Decl., ¶¶ 110–121). According to Petitioner, insulating material 30, which can be photosensitive or non-photosensitive organic material or inorganic material, also called a bank, is formed on both ends of electrode 28a (e.g., anode), which may be formed by an organic resin film or an insulating film including silicon. *Id.* at 43 (citing Ex. 1004, 11:22–65, Fig. 2).

Referencing the embodiment disclosed in Figure 15A of Yamazaki, Petitioner also argues that interlayer insulation film 1431 made of organic or inorganic material, e.g., a silicon nitride film, deposited below insulation film 1403, corresponds to insulation layer 30, and that an ordinarily skilled artisan would have understood this embodiment to teach an additional insulation layer 1431 formed under insulating material 1430. Pet. 43–44 (citing Ex. 1004, 35:65–36:54, Fig. 15A; Ex. 1002, Neikirk Decl., ¶ 115). Petitioner acknowledges that Anzai does not explicitly state what materials are used to form planarization layers 17 and 19 (other than organic resin for layer 17), but argues that Anzai discloses those layers function as the capacitance insulating film. Pet. 45 (citing Ex. 1003, 4:20–24, 5:62– 6:9). Petitioner also argues Anzai teaches that SiN can be used as interlayer insulating film 15 between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitor element 130 and in gate insulating film 12 between first and second capacitance layers 55, 54. Pet. 45 (citing Ex. 1003, 4:8–19, 4:17–24, 4:40–47, 5:62–6:9). According to Petitioner, an ordinarily skilled artisan would have understood that adding another insulating layer would improve the planarization of Yamazaki's

pixel area and would have had reason to add Anzai's planarization layer 19 above Yamazaki's insulating material 30 because both flatten the surface of the pixel area. *Id.* at 46 (citing Ex. 1003, 4:8–10, 4:17–24, Fig. 2A; Ex. 1004, 11:22–12:52, 20:17–39, Fig. 2; Ex. 1002, Neikirk Decl., ¶ 120). Petitioner adds that this modification to improve flattening would involve require only depositing another planarization layer on top of an already existing planarization layer using materials disclosed in both references and known methods. *Id.*

Patent Owner argues that, "as explained in Ground 1 [anticipation by Anzai] above, Anzai's planarization layer 19 is of an unknown material, so Petitioner has not proven that Anzai's planarization layer 19 is a 'capping layer' that is capable of protecting the layers underneath." PO Resp. 19. In a footnote, Patent Owner also asserts that "Petitioner's motivation to modify does not make sense. Why add another planarization layer if the insulating layer is already planarized? This would add manufacturing steps, complications, and cost. An additional layer would also reduce capacitance due to increased thickness." *Id.* at 19 n.1.

As we explained above with respect to claim 3, we find that Anzai does disclose a "capping layer," so we do not find contentions that Anzai's layer is unknown persuasive. We have reviewed Petitioner's arguments and evidence for claim 3 and find that Petitioner has shown by a preponderance of evidence that claim 3 would have been obvious over the combination of Yamazaki and Anzai.

4. Claim 4

With respect to claim 4, Petitioner cites Yamazaki's disclosure of SiN as a suitable material for insulation layer 30 as teaching the claimed feature

that at least one of the passivation layer (insulating material 30) and capping layer (planarization layer of Anzai) comprises SiN. Pet. 47 (citing Ex. 1004, 11:45–50; Ex. 1002, Neikirk Decl., ¶¶ 122–124).

Patent Owner reiterates its arguments that Anzai does not disclose a "capping layer," which we considered above. *See* PO Resp. 20. As we explained above, we do not find that argument to be persuasive. We have reviewed Petitioner's arguments and evidence for claim 4, and find that Petitioner has shown by a preponderance of the evidence that claim 4 would have been obvious over the combination of Yamazaki and Anzai.

5. Claim 7

Claim 7 depends from claim 1. Petitioner reads the limitations of claim 7 on Yamazaki and Anzai as follows:

> the second dielectric layer (Yamazaki's modified insulating material 30) comprises a passivation layer (Yamazaki's insulating material 30), a capping layer (Anzai's planarization layer 19) on the passivation layer and a second organic layer (Yamazaki's EL layer 31) formed on the capping layer, at least one of the passivation layer (insulating layer 30) and the capping layer (Yamazaki's insulating material 30) comprising silicon nitride, and the second organic layer (Yamazaki's EL layer 31) comprising the same material as the first organic layer (Yamazaki's EL layer 31).

Pet. 52 (citing Ex. 1002, Neikirk Decl., ¶ 136).

Patent Owner raises the same arguments considered above for claims 3 and 4. *See* PO Resp. 21; PO Sur-reply 24. For the reasons stated above, those reasons are not persuasive. We have reviewed Petitioner's evidence and arguments for claim 7 and find that Petitioner proved by a preponderance of the evidence that the combination of Yamazaki and Anzai teaches the limitations claim 7, and that there is a motivation to combine

Yamazaki and Anzai in the manner suggested with a reasonable expectation of success. Accordingly, we find that Petitioner has shown by a preponderance of the evidence that claim 7 would have been obvious over the combination of Yamazaki and Anzai.

IV. CONCLUSION

After considering the evidence and arguments presented in the Petition, we determine that Petitioner has established by a preponderance of the evidence that the challenged claims of the '121 patent are unpatentable as anticipated by Anzai, and obvious over the combinations of Anzai and Yamazaki and Yamazaki and Anzai, notwithstanding Patent Owner's arguments.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 318(a), claims 1–7 of the '121 patent have been shown to be unpatentable; and

FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.[6]

[6] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–3, 5	102(e)	Anzai	1–3, 5	
4	103(a)	Anzai, Yamazaki	4	
1–7	103(a)	Yamazaki, Anzai	1–7	
Overall Outcome			1–7	

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