Trials@uspto.gov
571-272-7822

Paper 35
Date: January 5, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00791
Patent 10,937,806 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL T. CYGAN, *Administrative Patent Judges.*

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318; 37 C.F.R. § 42.64

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition to institute an *inter partes* review of claims 8, 9, 11, and 12 of U.S. Patent No. 10,937,806 B2 ("the '806 patent," Ex. 1001). Paper 1 ("Pet."). Yangtze Memory Technologies Company, Ltd. ("Patent Owner") filed a Preliminary Response. Paper 10 ("Prelim. Resp."). On November 27, 2024, we instituted an *inter partes* review of all of the challenged claims based on all of the grounds identified in the Petition. Paper 11 ("Inst. Dec." or "Institution Decision"). Patent Owner filed a Response to the Petition (Paper 14, "PO Resp."), Petitioner filed a Reply (Paper 16, "Reply"), and Patent Owner filed a Sur-reply (Paper 18, "Sur-reply"). We held a consolidated oral hearing for this proceeding and IPR2024-00911 on September 4, 2025, and a transcript of the hearing has been entered into the record. Paper 29 ("Tr."). On November 24, 2025, a Good Cause Extension was issued to permit alignment with the schedule in IPR2024-00911. Papers 30, 31.

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). Based on the record before us, we conclude that Petitioner has not shown by a preponderance of the evidence that claims 8, 9, 11, and 12 of the '806 patent are unpatentable.

A. Real Parties in Interest

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as the real parties in interest. Pet. 5. Patent Owner identifies itself as the real party in interest. Paper 3 (Mandatory Notice), 2.

B. Related Matters

The parties indicate that the '806 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.). Pet. 5; Paper 3, 2. Claim 10 of the '806 patent, which depends on claim 8, is challenged in IPR2024-00911. Petitioner states it filed IPRs challenging other patents asserted in the district court cases, namely U.S. Patent Nos. 10,950,623 (IPR2024-00794), 10,658,378 (IPR2024-00788), 10,861,872 (IPR2024-00789), 10,868,031 (IPR2024-00790), 11,501,822 (IPR2024-00795), 11,468,957 (IPR2024–00792), and 11,600,342 (IPR2024-00793). Pet. 5–6.

C. The '806 Patent

The '806 patent, titled "Through Array Contact (TAC) for Three-Dimensional Memory Devices" relates to "a channel hole plug structure of three-dimensional (3D) memory devices and a method for forming the same." Ex. 1001, code (54), 1:18–20. An embodiment of the 3D memory device is illustrated in Figure 2 of the '806 patent and is reproduced below.

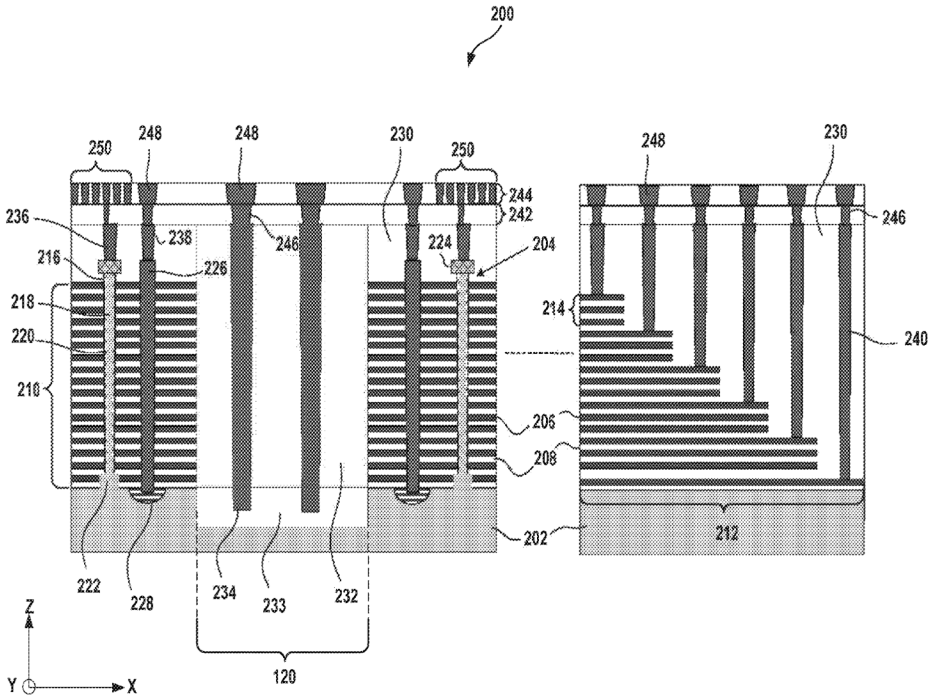


FIG. 2

Figure 2 "is a cross-sectional view of an exemplary 3D memory device 200" disclosed in the '806 patent. Ex. 1001, 3:41–42.

Memory device 200 can be a "NAND Flash memory device[1] in which memory cells are provided in the form of an array of NAND strings 204 extending vertically above substrate 202." *Id.* at 8:17–20. "The array device can include a plurality of NAND strings 204 that extend through a plurality of conductor layer 206 and dielectric layer 208 pairs" that alternate in the vertical direction, also referred to as "'alternating conductor/dielectric stack' 210." *Id.* at 8:20–31. Alternating conductor/dielectric stack 210 can include staircase structure 212, where each "level" or "step" 214 can include

[1] Though not explicitly defined in the specification, Petitioner's declarant states that "[t]he acronym 'NAND' refers to a 'not-AND' logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate." Ex. 1003 ¶ 42.

one or more conductor/dielectric layer pairs stacked. *Id.* at 8:54–59. "The top layer in each level 214 of staircase structure 212 is a conductor layer 206 available for interconnection in the vertical direction (e.g., along the z-axis)." *Id.* at 8:61–63. Figure 2 also shows "channel structure 216 that extends through alternating conductor/dielectric stack 210" that is filled with semiconductor materials and dielectric materials. *Id.* at 9:7–12. The embodiment illustrated in Figure 2 also includes slit structures 226 that also extend through alternating conductor/dielectric stack 210 and may extend along the y-axis to separate alternating conductor/dielectric stack into multiple blocks. *Id.* at 9:54–58.

Figure 2 also illustrates through array contacts ("TACs") 234, extending vertically through dielectric structure 232, which are within a TAC region 120 that can have, but are not limited to, a rectangle or square shape. *Id.* at 10:55–64. "TACs 234 can carry electrical signals from and/or to 3D memory device 200" and "can provide electrical connections between the 3D memory device 200 and the peripheral device." *Id.* at 11:8–14.

D. Illustrative Claim

Petitioner challenges claims 8, 9, 11, and 12 of the '806 patent. Claim 8, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

> 8. [1.PRE] A three-dimensional (3D) memory device, comprising:
>
> [8.A] an alternating conductor/dielectric layer stack;
>
> [8.B.i] a dielectric structure [8.B.ii] extending vertically through the alternating conductor/dielectric layer stack;
>
> [8.C] first and second channel regions comprising first and second pluralities of channel structures, respectively;

[8.D] slit structures extending vertically through the alternating conductor/dielectric layer stack;

[8.E] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[8.F] local contacts disposed on the first and second channel structures and the slit structures;

[8.G.i] a through array contact (TAC) region [8.G.ii] formed between the first and second channel regions, [8.G.iii] wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and

[8.H] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

Ex. 1001, 23:54–24:8 (bracketed material added).

E. Asserted Ground

Petitioner asserts that claims 8, 9, 11, and 12 would have been unpatentable on the following ground:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
8, 9, 11, 12	103[2]	Toyama[3]

Pet. 6–7. Petitioner presents three alternative arguments that claims 8, 9, 11, and 12 would have been obvious over Toyama, relying on different

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the '806 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

[3] Toyama, US Pub. No. 2017/0179026 A1, published June 22, 2017 (Ex. 1005).

structures and modifications to support each argument. *Id.* at 27–56 (alternative argument 1), 56–95 (alternative argument 2), 96–122 (alternative argument 3). Petitioner relies on the Declaration of Jack C. Lee, Ph.D. ("Lee Dec.," Ex. 1003) and the Reply Declaration of Dr. Jack C. Lee ("Lee Reply Dec.," Ex. 1043) in support of its contentions. Patent Owner relies on the declaration of Woodward Yang, Ph.D. ("Yang Dec." Ex. 2004). Transcripts of the depositions of Dr. Lee (Exs. 2006, 2008) and Dr. Yang (Ex. 1047) have been entered into the record.

II. ANALYSIS

A. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective evidence of obviousness or nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter*

partes review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon). Apart from limited circumstances not present here, this burden does not shift to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art ("POSITA") would have had "a bachelor of science degree in electrical engineering or a similar discipline" with "2–3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience)." Pet. 27 (citing Ex. 1003 ¶¶ 34–38). Petitioner further contends that a "POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled." *Id*.

Patent Owner does not object to Petitioner's proposed definition (PO Resp. 12), but Patent Owner's declarant Dr. Yang provides a slightly different definition, stating a POSITA:

> would have had at least a bachelor's degree in electrical engineering, materials science, or a similar discipline, along with at least 2 years of professional experience in semiconductor fabrication process integration for memory devices or an equivalent level of knowledge and experience. For example, an

> advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

Ex. 2004 ¶ 43.

Petitioner's proposed definition appears to be consistent with the cited prior art and the disclosure of the '806 patent, and we adopt it for purposes of this Decision. We note that our Decision would be the same under either definition of a POSITA.

C. Claim Construction

We construe claims challenged in an *inter partes* review proceeding, "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)," including construing the claims "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1348, 1375 (Fed. Cir. 2019).

The parties dispute the construction of the term "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" recited in claim element [8.G.iii].

1. [8.G.iii] " . . . a plurality of through array contacts (TACs) extending vertically through the dielectric structure"

Petitioner argues that the phrase "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" recited in claim element [8.G] encompasses multiple TACs, each extending through a separate, different dielectric structure, while Patent Owner argues that the phrase requires that the plurality of TACs (i.e., at least two TACs) must extend through the same dielectric structure. *See, e.g.*, Pet. 49–50; PO Resp. 18–21; Reply 2–4. In our Decision on Institution, we preliminarily construed this phrase to require that more than one (i.e., a plurality) TAC in the TAC region extends vertically through a single dielectric structure. *See* Inst. Dec. 17.

Based upon a full record, we construe this term of claim element [8.G.iii] (i.e., " . . . a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure") according to its plain language to require that a plurality (i.e., more than one) of TACs must extend vertically through a (i.e., at least one) dielectric structure. Under this construction, the plurality of TACs may extend through more than one dielectric structure, but the plurality of TACs must extend through at least one dielectric structure. The plain language of the claim is not satisfied if each TAC extends through a separate dielectric structure because, in this scenario, there is not *a plurality of TACs* that extend through a dielectric structure.

Petitioner asserts that because claim 8 uses an open-ended transitional phrase ("comprising") and an indefinite article ("a") preceding "dielectric structure," the claim encompasses a device with multiple dielectric

structures. Pet. 32 n.4 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) and stating that the indefinite articles "a" or "an" means "one or more"). We agree with Petitioner that the disputed claim language permits plural (i.e., more than one) dielectric structures. However, the plain language of the claim still requires that a *plurality* of TACs extend through a dielectric structure. For example, if a memory device had two dielectric structures labeled A and B, element [8.Giii] would be met if the *plurality* of TACs extended through at least one (or more than one) of the dielectric structures, (i.e., the plurality of TACs could extend through either structure A or structure B or both structures A and B). Element [8.G.iii], however, would not be met if one TAC extended through only dielectric structure A and a separate TAC extended through only dielectric structure B because, in this example, a *plurality* of TACs did not extend through at least one dielectric structure.

In its Reply, Petitioner points to, *inter alia*, the *Baldwin* decision, in which the Federal Circuit held that "*a* pre-soaked fabric roll . . . , said fabric roll having a sealed sleeve" was not limited to a single pre-soaked fabric roll but would encompass multiple fabric rolls in contact with the same plastic sleeve. Reply 4–5 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1343 (Fed. Cir. 2008) (emphasis added, alteration in original)). We agree that the article "*a*" does not limit the dielectric structure to a single dielectric structure. However, unlike *Baldwin*, which relates to "*a* pre-soaked fabric roll" and "*a* sealed sleeve" element [8.G.iii] refers to "a *plurality*" of TACs. The plain language of the term requires that a plurality of TACs extend through one (or more than one) dielectric structure. Petitioner's proposed construction would read "*a plurality*" out of the claim language.

Our construction is consistent with the Specification of the '806 patent, which discloses a plurality of TACs extending through a single dielectric structure and does not disclose multiple TACs, each extending through a different dielectric structure. *See generally* Ex. 1001; *see also e.g.*, *id.* at Figs. 1B, 1C, 2, 12, 13 (each depicting multiple TACs extending through the same dielectric structure). Petitioner cites to language in the Specification that states "terms, such as "a," "an," or "the" . . . "may be understood to convey a singular usage or to convey a plural usage depending at least in part upon context." Reply 3 (citing Ex. 1001, 4:17–25). This language does not change our analysis. As noted above, we agree that "a" dielectric structure or "the" dielectric structure is not limited to a single dielectric structure. However, even if the use of the article "a" or "the" with "dielectric structure" permits for one or more than one dielectric structure, this does not change the claim language that requires a *plurality of TACs* to extend through the either one or the more than one dielectric structure(s). The Federal Circuit has explained that even if use of an indefinite article in a claim may "allow for more than a single instance of the claim element, [the claim language] may nonetheless require that a single instance of the element be capable of performing all the recited functionality." *See Salazar v. AT&T Mobility LLC*, 64 F.4th 1311, 1317 (Fed. Cir. 2023). Thus, although we agree that the claim permits more than one dielectric structure, the claim language expressly requires that a plurality of TACs extend through the dielectric structure, thus indicating that more than one TAC must pass through each dielectric structure.

Petitioner also states the '806 patent "contemplates embodiments with multiple dielectric structures (each of which includes a single TAC)." Reply 3 (citing Ex. 1001, 21:11–28; Ex. 1043 ¶¶ 12–15). Petitioner's arguments

are not persuasive because they fail to address the claim language that requires "*a plurality of TACs*" to extend to through a dielectric structure. Indeed, Dr. Lee does not address the full scope of the claim language in his analysis as he only discusses "the phrase 'through array contacts'" and not "a plurality of through array contacts" as recited in the claim. *See* Ex. 1043 ¶ 10 (stating that "the phrase 'through array contacts' may refer to contacts that extend vertically through multiple dielectric structures"); *see also id.* ¶¶ 11–15 (not addressing the "plurality" requirement of claim 8). Petitioner does not persuasively explain how this portion of the Specification relates to construction of the particular term at issue that requires a plurality of TACs to extend through the dielectric structure.

No other terms require express construction to resolve any issue in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see also Nidec Motor Corp. v. Zhongshan Board Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

D. Obviousness over Toyama (Ex. 1005)

As noted above, Petitioner presents three alternative arguments that claims 8, 9, 11, and 12 would have been obvious over Toyama. Pet. 27–56 (alternative argument 1), 56–95 (alternative argument 2), 96–122 (alternative argument 3). We address each argument in turn, and, for the following reasons, we determine that Petitioner has not shown by a preponderance of the evidence that claims 8, 9, 11, or 12 would have been obvious over Toyama under any of the alternative arguments.

1. Overview of Toyama

Toyama is titled "Through-Memory-Level Via Structures for a Three-Dimensional Memory Device." Ex. 1005, code (54). Toyama relates to

three-dimensional NAND memory devices, such as vertical NAND strings, and describes four exemplary structures and modifications thereof. *Id.* ¶¶ 4, 14–155 (describing figures depicting first, second, third, and fourth exemplary structures as well as various modifications of those structures).

Embodiments of Toyama's "first exemplary structure" are illustrated in Figures 1 through 17. *See* Ex. 1005 ¶¶ 14–49, 163–260, Figs. 1–17. Figure 15A is shown below. *Id.* ¶ 39.

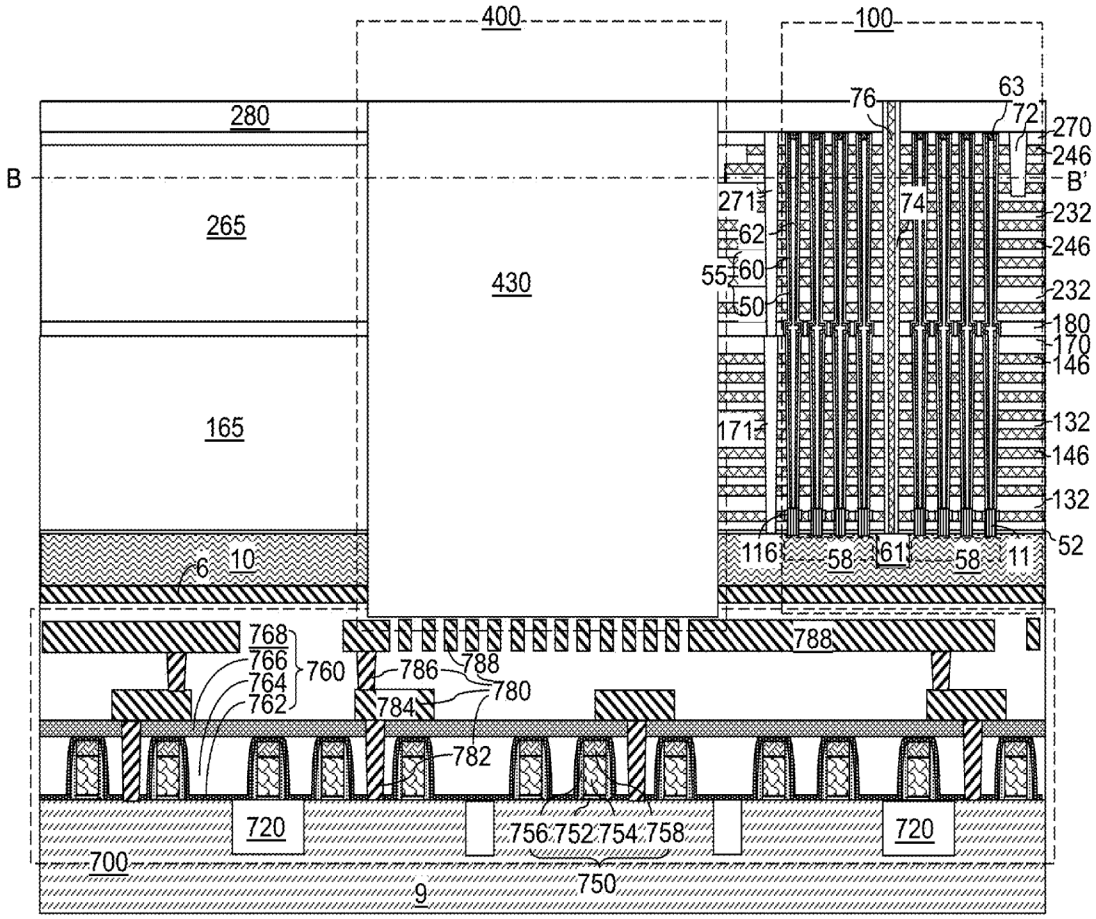


FIG. 15A

Figure 15A is a vertical cross-sectional view of the first exemplary structure

of the first embodiment after formation of, *inter alia*, electrically conductive layers. Ex. 1005 ¶ 39.

At least one dielectric layer 760 is formed over the semiconductor devices, and lower level metal interconnect structures 780 formed thereon to function as landing pads for through-memory-level via structures. Ex. 1005 ¶ 164. Upon these structures in underlying peripheral region 700 (those having numbers in the 700s), a planar semiconductor layer 10 is formed. On semiconductor layer 10 is an alternating stack of conductive layers 146, 246 (replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 172, 196, 228. In portions of the alternating stack, supporting pillar structures 171 are formed, and other portions of the dielectric stack appear as a stepped region. *Id.* ¶ 182, Fig. 4B. In the stepped region, a through-memory-level opening 769 can extend from the top of the device down to the lower level metal interconnect structures 780 in peripheral region 700. *Id.* ¶ 213. A dielectric fill material portion 430 is formed within each through-memory-level opening 769. *Id.* ¶ 216.

Figures 17E and 17F illustrate an exemplary layout of the upper level metal interconnect structures. *Id.* ¶ 251. In this embodiment, some upper level metal interconnect structures 108 are electrically coupled to the lower level metal interconnect structures 780 by the through-memory-level via structures 488 located in region 400 and are electrically coupled to the word lines 46 by the word line contact via structures 86 in region 200. *Id.*

Toyama also describes a "second modification of [a] fourth exemplary structure" ("Second Modification") illustrated in Figures 44A through 49. Ex. 1005 ¶¶ 93–103. Figure 49 is shown below:

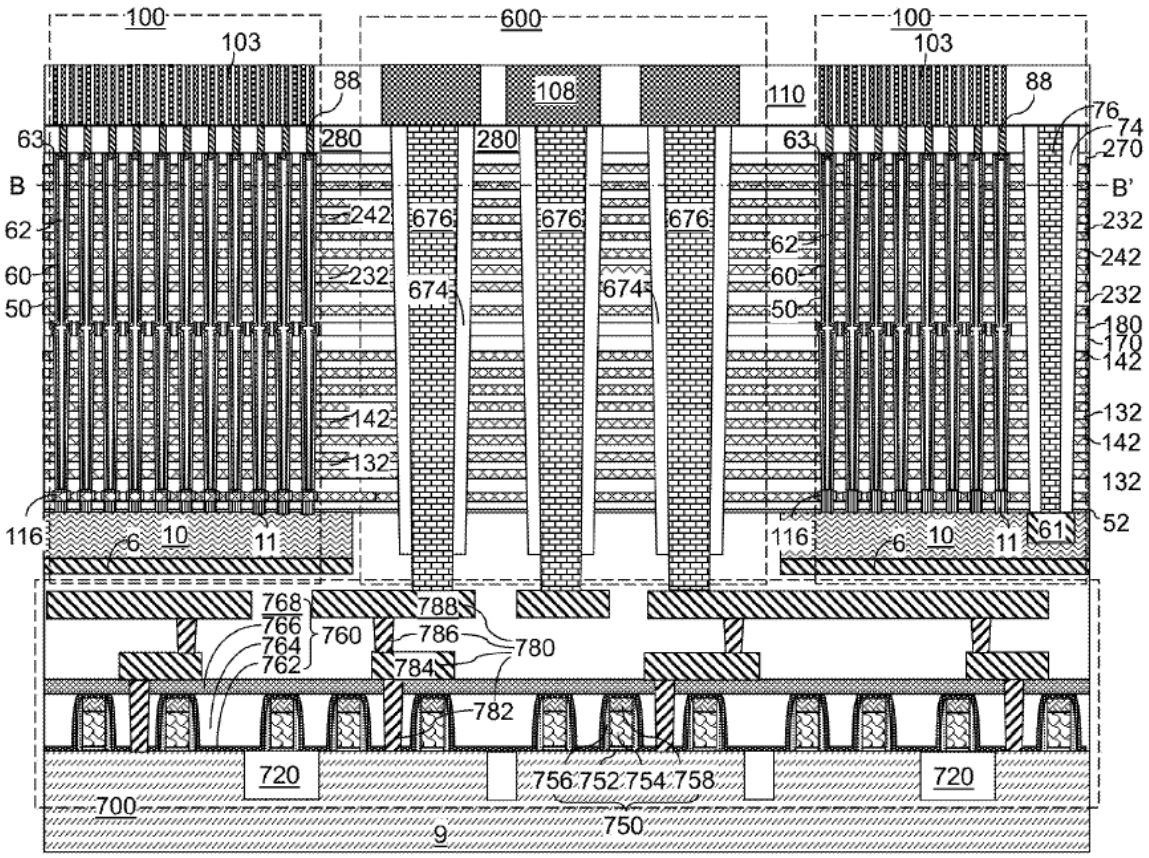


FIG. 49

Figure 49 is a vertical cross-sectional view of Toyama's second modification of its fourth exemplary structure after formation of upper level metal interconnect structures. Ex. 1005 ¶ 103. Figure 49 depicts semiconductor substrate 9 having peripheral region 700, upon which planar semiconductive layer 10 is formed having an alternating stack of conductive layers 146, 246 (replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 310–311, 332. Multiple through-memory-level openings 676, surrounded by insulating liners 674, are created within the alternating stack. *Id.* ¶¶ 339–341.

2. Asserted Obviousness over Toyama's Second Modification to its Fourth Exemplary Structure (Alternative Argument 1)

Petitioner argues that claims 8, 9, 11, and 12 would have been obvious over Toyama's Second Modification (i.e., the second modification to Toyama's fourth exemplary structure). Pet. 27–56; Reply 6–13. Patent Owner opposes. PO Resp. 17–25; Sur-reply 3–16. In our Institution Decision, we determined that Petitioner failed to show a reasonable likelihood that claims 8, 9, 11, or 12 would have been obvious over Toyama's Second Modification. Upon review of the full record, for the reasons stated below, we determine that Petitioner has not shown by a preponderance of the evidence that Toyama's Second Modification teaches all limitations of claim 8 and, therefore, has not shown that claim 8, or claims 9, 11, or 12 which depend therefrom, would have been obvious over Toyama's Second Modification.

(a) Claim 8

Petitioner contends that Toyama's Second Modification discloses or suggests all elements of independent claim 8. Pet. 27–54. For example, Petitioner asserts that Toyama's Second Modification is a "three-dimensional non-volatile memory device[]" having an "alternating stack (132, 146, 232, 246)" of "electrically conductive layers" and "insulating layers" as recited in the preamble and claim element [8.A]. *Id.* at 28–29 (citing Ex. 1005 ¶¶ 156, 337, 340, Figs. 45A, 46A, 49; Ex. 1003 ¶¶ 86–89). Petitioner also asserts that Toyama's Second Modification teaches a "dielectric structure" (insulating liners 674) "extending vertically through the alternating conductor/dielectric layer stack" (alternating conductor/dielectric stack (132, 146, 232, 246)) as recited in claim element [8.B]. *Id.* at 29–33 (citing, *inter alia*, Ex. 1005 ¶¶ 223, 338–340, 381,

Fig. 49; Ex. 1003 ¶¶ 91–94, 97). Petitioner asserts that Toyama discloses "first and second channel regions" (first and second parts of memory array region 100) "comprising first and second pluralities of channel structures" (first and second pluralities of memory stack structures 55) as required by claim element [8.C]. *Id.* at 33–36 (citing Ex. 1005 ¶¶ 210, 323–333, 388 Fig. 48B, 49; Ex. 1003 ¶¶ 98–99). Petitioner maps Toyama's "laterally-elongated contact via structures 76" that extend vertically through alternating stack (132, 146, 232, 246) to "slit structures extending vertically through the alternating conductor/dielectric layer stack" as recited in claim element [8.D]. *Id.* at 36–39 (citing, *inter alia*, Ex. 1005 ¶¶ 237, 241, 318–320, Figs. 48B, 49; Ex. 1003 ¶¶ 102–104). Petitioner also maps Toyama's staircase regions, which contain "conductor layer[s]," shown in Figure 17C to "a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon" recited in claim element [8.E]. *Id.* at 39–41 (citing Ex. 1005 ¶ 232, Fig. 17C; Ex. 1003 ¶¶ 105–107); *see also id.* at 41 (stating a POSITA would have understood that Toyama's Second Modification also teaches the above citations to Toyama's first exemplary structure, depicted in Figure 17C). Claim element [8.F] recites "local contacts disposed on the first and second channel structures and the slit structures." Petitioner asserts that Toyama's "drain contact via structures 88" contacting or extending above the "memory stack structures 55" disclose the recited "local contacts disposed on the first and second channel structures." *Id.* at 41–42 (citing Ex. 1005 ¶ 251, Fig. 49; Ex. 1003 ¶ 109). Petitioner admits that Toyama does not expressly disclose local contacts (source connection via structures 91) disposed on the slit structures ("laterally-elongated contact via structures 76"), but asserts that a POSITA

would have understood that Toyama's Second Modification includes, or would have rendered obvious, local contacts disposed on the slit structures (source connection via structures 91) to provide a higher-level source connection in order for via structures to serve as source lines for source region 61. *Id.* at 43–44 (citing Ex. 1005 ¶¶ 250, 342, 382; Ex. 1003 ¶¶ 110–112).

With respect to claim element [8.G.i]–[8.G.ii], Petitioner asserts Toyama's Second Modification, shown in Figure 49 below, depicts a "through array contact (TAC) region" (part of through-memory-level via region 600)[4] that is "formed between first and second channel regions" (first and second parts of memory array region 100). *Id.* at 44–48 (citing Ex. 1005, ¶¶ 334, 378, Figs. 48B, 49; Ex. 1003 ¶¶ 113–114, 116–117).

[4] The "through-memory-level via region 600" in Toyama contains the "through-memory-level via structures 676," which Petitioner maps to the TAC region and TACs, respectively. *See* Pet. 44–46.

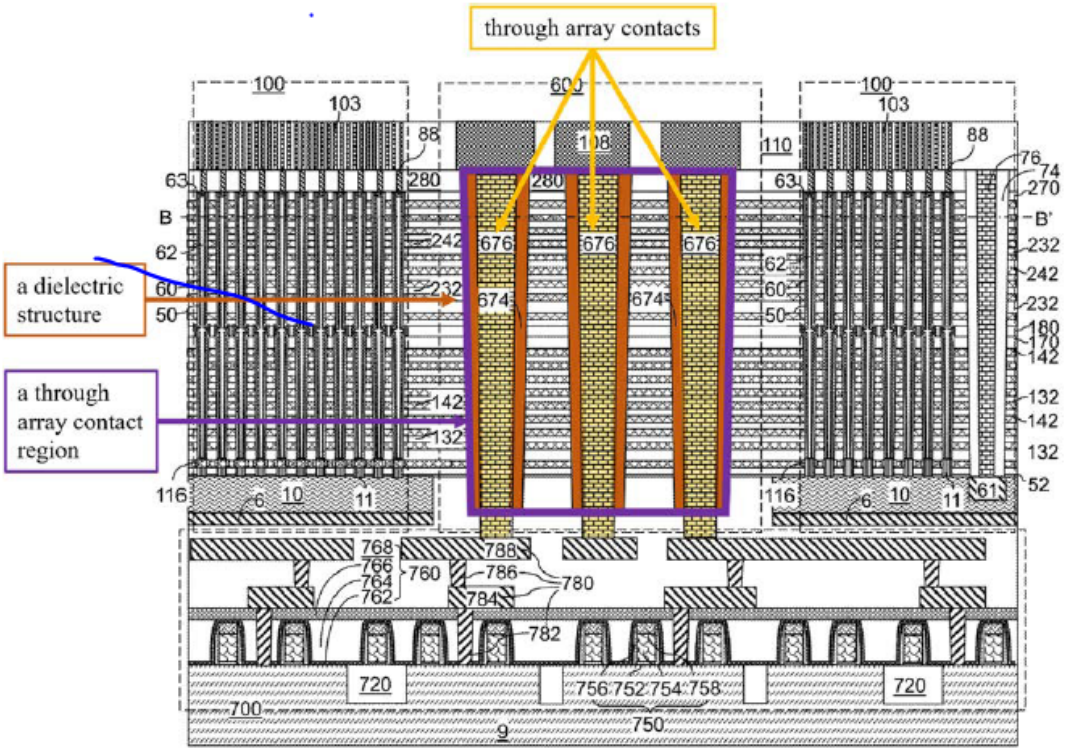


FIG. 49

Toyama's Figure 49 above, with Petitioner's annotations added, depicts though-memory-level via structures 676 (yellow), insulating liners 674 (orange), and through-memory-level via region 600. *See* Pet. 50; Ex. 1005 ¶¶ 341–342, Fig. 49). Petitioner also asserts that Toyama's through array contacts (though-memory-level via structures 676 (yellow)) are a plurality of TACs that "extend vertically through the dielectric structure" (insulating liners 674 (orange)) as required by claim element [8.G.iii]. Pet. 49–50 (citing Ex. 1005 ¶¶ 341–342, Fig. 49; Ex. 1003 ¶¶ 114–115).

Lastly, Petitioner argues that Toyama's "dummy memory stack structures 55D" surrounding the "through-memory-level via region 600" between the "first and second parts of 'memory array region 100'" disclose a "plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions" as recited in claim element [8.H]. *Id.* at 51–54 (citing Ex. 1005 Fig. 48; Ex. 1003 ¶ 118).

Petitioner also states that claim 8 does not require non-electrically functional channel structures on four sides of the TAC region, but that a POSITA would have understood (1) that Toyama's dummy memory stack structures 55D encircle Toyama's TAC region or (2) that it would have been obvious to do so. *Id.* at 52–54 (citing Ex. 1005 ¶¶ 182, 333, Fig. 48B; Ex. 1003 ¶¶ 120–121).

(1) Analysis

Based upon our review of the full record we determine that Petitioner has not sufficiently shown that Toyama teaches or suggests a plurality of TACs extending vertically through the dielectric structure as required claim element [8.G.iii]. As noted above, we construe the phrase "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" to require that *a plurality* of TACs (i.e., more than one TAC) must extend through the same, at least one, dielectric structure. Petitioner asserts that Toyama's "through-memory-level via structures 676" (the asserted TACs) extend through "insulating liners 674" (the asserted dielectric structure). *See, e.g.,* Pet. 49–50 & n.8 (citing Ex. 1005 ¶¶ 341–342, Fig. 49; Ex. 1003 ¶¶ 114–115). However, in this embodiment, each TAC extends through only one dielectric structure (i.e., liner 674) and, therefore, does not teach a *plurality* of TACs extending through a dielectric structure. Thus, Toyama does not teach claim element [8.Giii] under our adopted claim construction.

In its Petition, Petitioner also argues that Toyama's "'insulating liners 674' are individually and collectively a dielectric *structure* because "these components together are something 'that is constructed." Pet. 31–32 (citing Ex. 1021 (Merriam-Webster dictionary), 4 (defining structure as, *inter alia*, "something ([such] as a building) that is constructed"); Ex. 1003 ¶ 94).

Dr. Lee also states that under its plain and ordinary meaning, a structure is something that is constructed and the dielectric liners are constructed together and have the same insulating and isolating function. Ex. 1003 ¶ 94.

Petitioner does not persuade us that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure. Every component of Toyama's memory device is something that is constructed. The dictionary definition "something . . . that is constructed" relied upon by Petitioner uses the context of "a building"; i.e., a single thing, that is constructed. Ex. 1021, 4, 5 ("2a : something (as a building) that is constructed").

In its Reply, Petitioner further asserts that, even under the Board's adopted construction, Toyama's insulating liners 674 are "collectively a single *dielectric structure*." Reply 7–11 (citing Pet. 32–33; Ex. 1043 ¶¶ 17–19). Citing a new definition of "structure" as "something arranged in a definite pattern of organization," Petitioner asserts that Toyama's insulating liners 674 *collectively* are a dielectric structure because the term "structure" does "not require all elements of the structure to be contiguous." *Id.* at 8 (citing Ex. 1021, 4 (defining a structure as "[2]b : something arranged in a definite pattern of organization <a rigid totalitarian>"). To support its argument that Toyama's non-contiguous, insulating liners collectively are a structure, Petitioner points to photographs of a "wall" made up of "wooden posts" (Ex. 1045) and a "staircase" made up of "floating stairs" that are each attached to the wall (Ex. 1046). *Id.* at 8–11. Petitioner asserts that, just like a "wall" made up of wooden posts that do not touch each other, and a "staircase" made up of individual stairs that do not touch each other, Toyama discloses individual insulating liners 674 that collectively are a single dielectric structure. *Id.* at 8–11 (citing Ex. 1044, 45:3–4, 47:3–6;

Ex. 1043 ¶¶ 18–19). Petitioner asserts that, like the wall posts and stairs in the photos, each of Toyama's insulating liners 674 are arranged in a definite pattern of organization and therefore Toyama's insulating liners are individually and collectively a dielectric structure. *Id.* at 8, 11 (stating that all the liners have the same function of insulating TACs).

We disagree with Petitioner's arguments. Even if a wall can be made up of non-contiguous wooden posts or a staircase can be made up of individual, non-contiguous stairs, we fail to see how this argument supports a finding that a *single dielectric structure* is made up of *multiple dielectric structures*. Significantly, Petitioner does not argue that a single wall can be made up of multiple, non-contiguous walls or that a single staircase can be made up of multiple, non-contiguous staircases. Nor does Petitioner argue that a single wooden post is made up of multiple wooden posts or that a single stair is made up of multiple stairs. As such, we disagree that Toyama's multiple, non-contiguous dielectric structures collectively make up a single dielectric structure.

(2) Conclusion

After considering Petitioner and Patent Owner's positions and supporting evidence, we are not persuaded that Petitioner sufficiently demonstrates that Toyama's Second Modification teaches or suggests a "plurality of through array contacts (TACs) extending vertically through the dielectric structure" as recited in independent claim 8. Accordingly, we determine that Petitioner does not show by a preponderance of the evidence that claim 8 would have been obvious over Toyama's Second Modification.

(b) Claims 9, 11, and 12

Claims 9, 11, and 12 depend, directly or indirectly, from claim 8. Ex. 1001, 24:9–11, 24:21–24. Petitioner asserts that Toyama's Second

Modification teaches or suggests the limitations of these dependent claims. Pet. 54–56. None of Petitioner's arguments remedy the deficiency set forth above regarding independent claim 8. Accordingly, for the same reasons given above with respect to Petitioner's challenge of claim 8, we also conclude that Petitioner does not demonstrate by a preponderance of the evidence that claims 9, 11, or 12 would have been obvious over the teachings of Toyama.

3. Asserted Obviousness over Toyama's First Exemplary Structure (Alternative Argument 2)

Petitioner contends that claims 8, 9, 11, and 12 would have been obvious over Toyama's first exemplary structure ("First Exemplary Structure"). Pet. 56–95; Reply 13–21; PO Resp. 25–37; Sur-reply 16–24. Patent Owner opposes. In our Institution Decision, we determined that Petitioner showed a reasonable likelihood of showing that at least claim 8 would have been obvious over Toyama's First Exemplary Structure. Upon review of the full record, for the reasons stated below, we determine that Petitioner has not shown by a preponderance of the evidence that claims 8, 9, 11, or 12 would have been obvious over Toyama's First Exemplary Structure.

(a) Claim 8

Petitioner contends that Toyama's First Exemplary Structure[5] teaches or renders obvious all elements of independent claim 8. Pet. 56–94. For example, Petitioner asserts that Toyama discloses a three-dimensional non-volatile memory device having an alternating conductor/dielectric layer stack ("alternating stack (132, 146, 232, 246)") as recited in the preamble

[5] Toyama's First Exemplary Structure is depicted in Figures 1–17 of Toyama. *See* Ex. 1005 ¶¶ 14–49.

and claim element [8.A]. *Id.* at 56–57 (citing Ex. 1005 ¶¶ 156, 172, Fig. 17A; Ex. 1003 ¶ 128). Petitioner asserts that the upper part of "dielectric fill material portion 430" shown in Toyama's Figure 15A (shown below) is a dielectric structure that extends vertically through alternating conductor/dielectric stack, (elements 132, 146, 232, 246 highlighted in green and yellow) as required by claim element [8.B]. *Id.* at 59–64 (citing, *inter alia*, Ex. 1005, 126, 173, 190, 213, 216, Figs. 10A, 15A, 16B; Ex. 1003 ¶¶ 130–135).

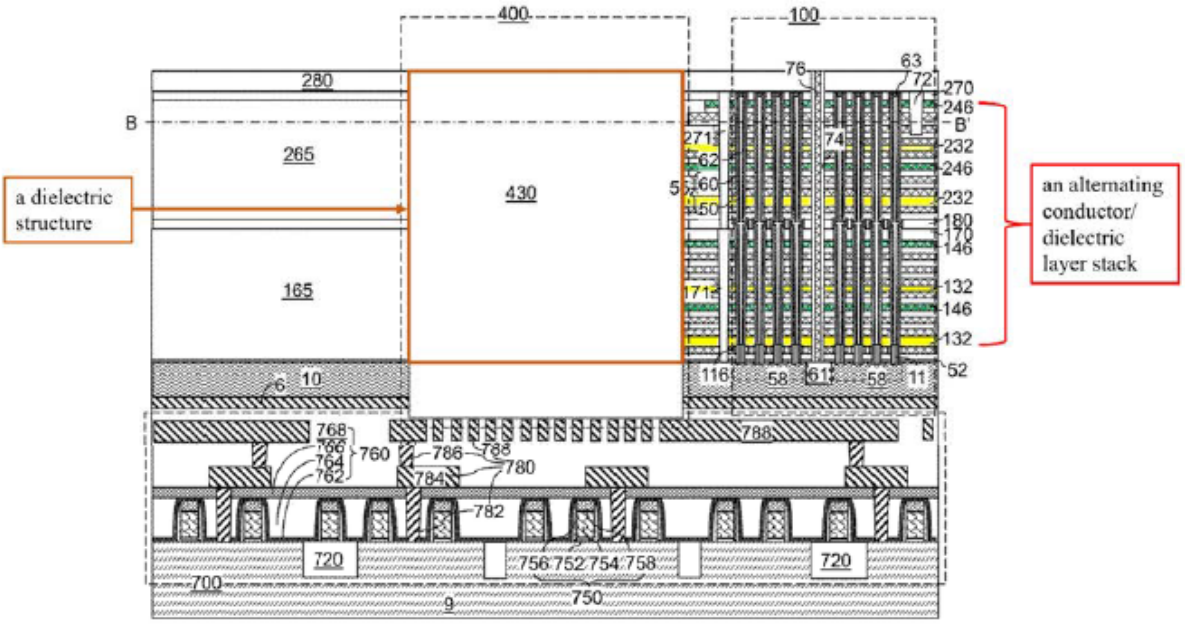


FIG. 15A

Toyama's Figure 15A above, with Petitioner's annotations added, "is a vertical cross-sectional view of the first exemplary structure after formation of electrically conductive layers, insulating spacers, and backside contact via structures." Pet. 60; Ex. 1005 ¶ 39, Fig. 15A.

Claim element [8.C] requires that the memory device have "first and second channel regions comprising first and second pluralities of channel structures, respectively." Petitioner asserts that Toyama's First Exemplary Structure depicted in Figure 16B, reproduced below, has a channel region

(part of "memory array region 100") comprising channel structures ("memory stack structures 55"). *See* Pet. 64–66 (citing Ex. 1005 ¶¶ 49, 203, Figs. 16B, 17A, 17E; Ex. 1003 ¶¶ 136, 137).

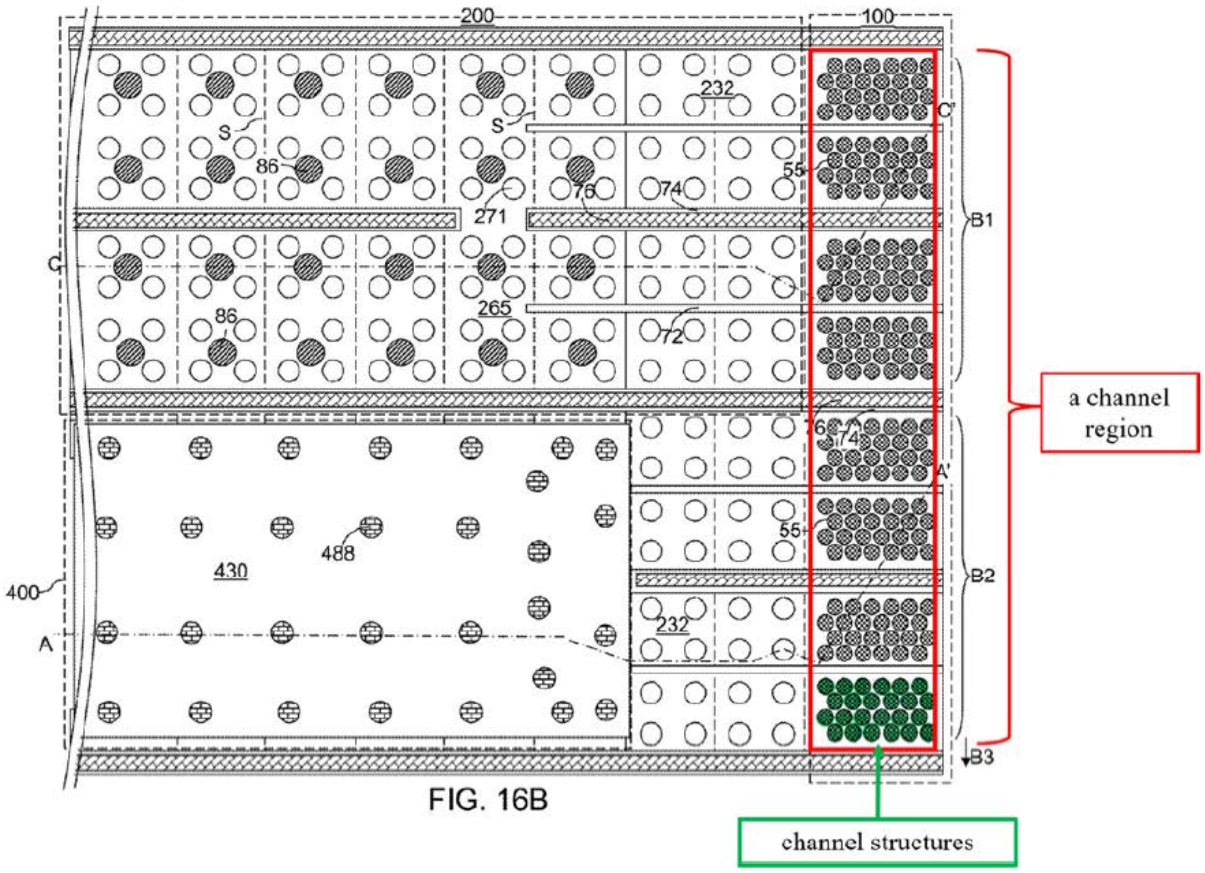
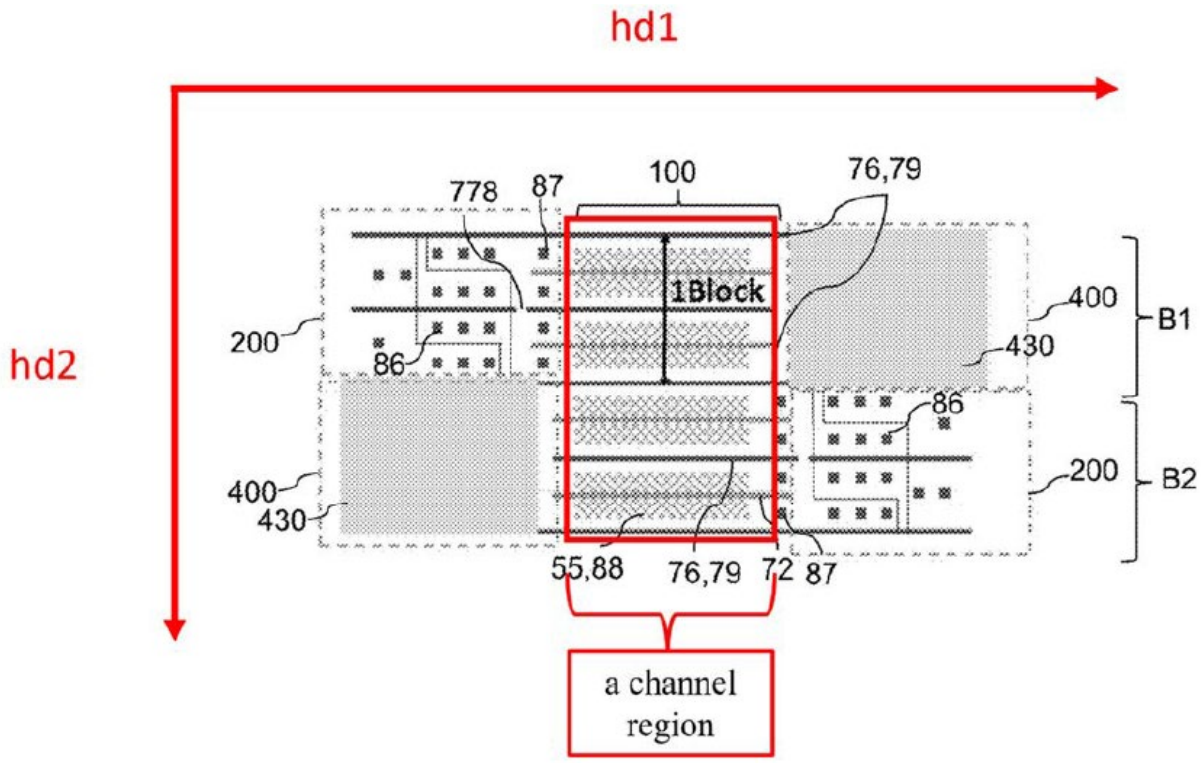


FIG. 16B

Toyama's Figure 16B, with Petitioner's highlighting added, is a horizontal cross-sectional view of the first exemplary structure depicting memory stack structures 55 (green) and memory array region 100 (red). Ex. 1005 ¶ 43, Fig. 16B; Pet. 66.

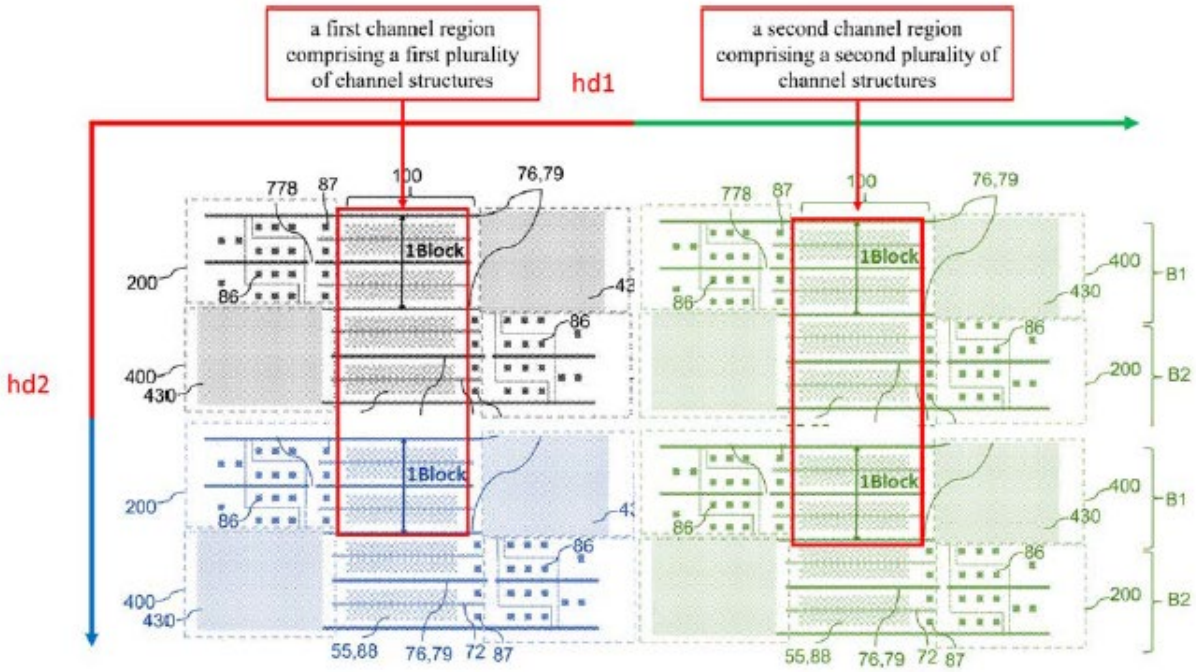
Petitioner further asserts that memory array region 100 (red) in Toyama's Figure 17E, reproduced below, is also a channel region.



Toyama's Figure 17E, with Petitioner's annotations added, is a top-down view of an alternative exemplary structure according to the first embodiment of the present invention, that Petitioner asserts may be used with Toyama's first exemplary structure. Ex. 1005 ¶ 49; Pet. 66–67.

Petitioner asserts that Toyama expressly contemplates that the layout shown in Figure 17E repeats in the hd2 (up-down) direction. Pet. 67–68 (citing Ex. 1005 ¶ 220; Ex. 1003 ¶ 138), 78 (citing Ex. 1003 ¶ 154). Petitioner admits that "Toyama does not expressly repeat the layout shown in Fig. 17E in the hd1 (i.e., left-right) direction" but that "a POSITA would have found it obvious to do so." *Id.* at 68. In particular, Petitioner asserts that because a POSITA would have found it obvious to implement Toyama's first exemplary structure in a 3D memory device with multiple planes, that "a POSITA would have found it obvious to repeat the layout shown in

Fig. 17E in the hd1 ***and*** hd2 directions, as shown in the modified figure below." *Id.* at 69 (citing Ex. 1005, Fig. 17E (modified)).



Petitioner's Modified Figure 17E depicts the layout of Figure 17E repeated in both the hd1 (left-right) and hd2 (top-down) direction. *See* Pet. 68–69; *see also id.* at 78 (stating modified Figure 17E depicts, on the left side (red), a first channel region comprising a first plurality of channel structures and on the right side (red), a second channel region comprising a second plurality of channel structures as required by claim element [8.C]).

Petitioner contends that a POSITA would have known to implement a flash memory device in multiple planes, each including a distinct memory array region and a staircase structure, by "placing the planes beside each other" in the left-right direction. *See id.* at 69–70 (citing, *inter alia*, Ex. 1003 ¶¶ 141–143; Ex. 1023, 247). To support this argument, Petitioner provides examples of flash memory devices with multiple planes. *Id.* at 70–73 (citing Ex. 1024, 13:37–44; Ex. 1023, 144, Fig. 6.1; Ex. 1014, 313–

314, Figs. 7.26, 7.35). Petitioner states a POSITA would have known the benefits of a multi-plane flash memory device, such as multiple planes make it "possible to issue a read command on multiple planes simultaneously," "can improve [write] throughput," and "improve the performance of NAND based systems." *Id.* at 74–75 (citing Ex. 1003 ¶¶ 141–147; Ex. 1025, 42, 44–45, 171, Fig. 2.19, 2.24).

Petitioner also asserts that a POSITA would have had a reasonable expectation of success in implementing multiple planes of Toyama's first exemplary structure in the hd1 direction because NAND flash memory devices with multiple planes existed for many years before the priority date of the '806 patent and repeating the layout in Figure 17E for each plane would have been straightforward and predictable. *Id.* at 76–77 (citing Ex. 1003 ¶ 151); *see also id.* at 71–75 (providing examples of multi-plane flash memory devices). Dr. Lee testifies that this modification is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance). *See, e.g.*, Ex. 1003 ¶ 151.

With respect to claim element [8.D], Petitioner asserts that Toyama's laterally-elongated contact via structures 76 are the "slit structures" that extend vertically through the alternating conductor/dielectric layer stack ("alternating stack 132, 146, 232, 246"). Pet. 79–80 (citing Ex. 1005, Fig. 17A, 17B; Ex. 1003 ¶¶ 154–156). Petitioner also asserts that Toyama discloses staircase regions (a "staircase structure") that is disposed in alternating stack 132, 146, 232, 246 (an "alternating conductor/dielectric stack layer") as required by claim element [8.E]. *Id.* at 80–81 (citing Ex. 1003 ¶ 157; Ex. 1005, Fig. 17C). Petitioner also contends that Toyama

discloses local contacts ("drain contact via structures 88") disposed on (in contact with and extending above) the channel structures ("memory stack structures 55"), and local contacts ("source connection via structures 91") disposed on (above) the slit structures ("laterally-elongated contact via structures 76") as recited in claim element [8.F]. *Id.* at 81–82 (citing Ex. 1005 ¶ 251, Fig. 17A; Ex. 1003 ¶¶ 158–159).

Claim elements [8.G.i]–[8.G.ii] require a "through array contact (TAC) region formed between the first and second channel regions." Ex. 1001, 24:1–2. Petitioner admits that Toyama's First Exemplary Structure does not expressly disclose a TAC region (part of "through-memory-level via region 400") that is formed between the first and second channel regions. Pet. 85; *see also* Ex. 1005, Fig. 17A (depicting a channel region on only one side of the asserted TAC region). Petitioner, however, asserts, "as explained for limitation [8.C] above, a POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure in the hd1 direction." Pet. 85 (citing Pet. 69–77). Petitioner asserts "[t]hus, as depicted in the modified figure [17E] . . . , Toyama renders obvious *a through array contact (TAC) region* (part of 'through-memory-level via region 400') *formed between the first and second channel regions* (first and second 'memory array regions 100')." *Id.* at 85–86 (citing Ex. 1005 Fig. 17E; Ex. 1003 ¶¶ 165–166) (color emphasis omitted); *see also* Reply 17–20.

For claim element [8.G.iii], Petitioner asserts that Toyama teaches a "TAC region" (part of though-memory-level region 400) that "comprises a plurality of through array contacts (TACs)" (through-memory-level via structures 488) "extending vertically through the dielectric structure" (dielectric fill 430). Pet. 86–87 (citing Ex. 1005 ¶ 239, Fig. 17A; Ex. 1003

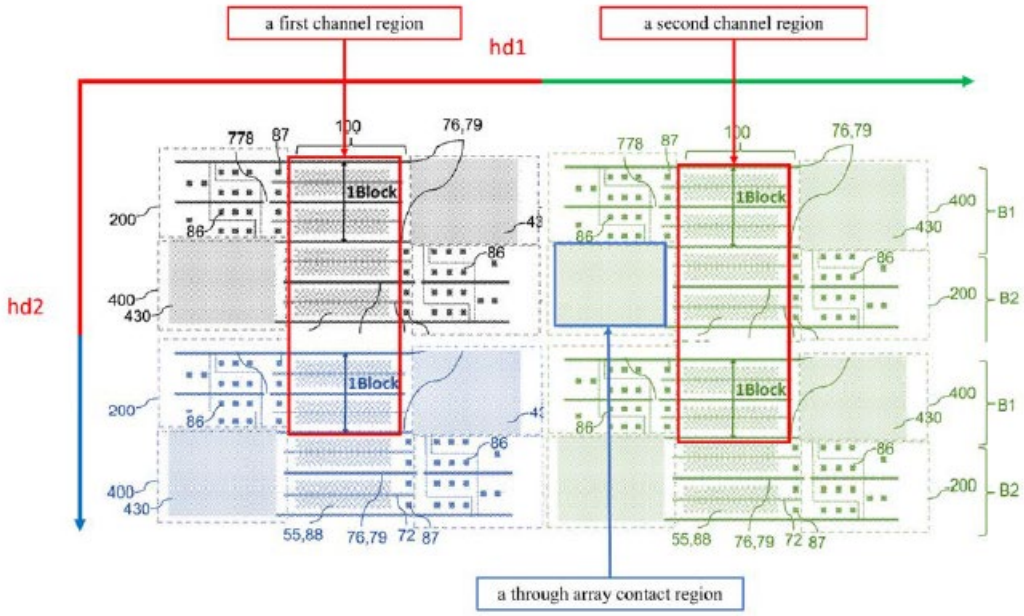
¶¶ 162–163; Pet. 57–64, 83–85). With respect to claim element [8.H], Petitioner asserts that Toyama's first- and second-tier support pillar structures (171, 172) are a "plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions." *Id.* at 86–93 (citing Ex. 1005 ¶¶ 182, 197, 203, 311, Figs. 16B, 17A, 17E; Ex. 1003 ¶¶ 168–173, 178; Ex. 1016 ¶ 162; Ex. 1017, 9:50–67; Ex. 1015 ¶¶ 73–81).

(1) Analysis

As noted above, in our Decision on Institution, we determined that Petitioner provided sufficient argument and evidence to show a reasonable likelihood of showing that claim 8 would have been obvious over Toyama's First Exemplary Structure. Inst. Dec. 28–29. We noted that Patent Owner's arguments that a POSITA would not modify Toyama to repeat in the hd1 (left-right) direction raised factual issues that are best resolved on a full record. *Id.* Based on our review of the complete trial record, we determine that Petitioner fails to establish by a preponderance of the evidence that a POSITA would have modified Toyama to implement multiple planes of Toyama's first exemplary structure in the hd1 (left-right) direction, and thus, does not show by a preponderance of the evidence that the proposed modification teaches all of the limitations of claim 8.

Claim elements [8.G.i]–[8.G.ii] require a "through array contact (TAC) region formed between the first and second channel regions." Ex. 1001, 24:1–2. Petitioner admits that Toyama's First Exemplary Structure does not expressly disclose a TAC region (part of "through-memory-level via region 400) that is formed between the first and second channel regions. Pet. 85; *see also* Ex. 1005, Fig. 17A (depicting a channel region on only one side of the asserted TAC region). Petitioner, however,

asserts, "as explained for limitation [8.C] above, a POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure in the hd1 direction." Pet. 85 (citing Pet. 69–77). "Thus, as depicted in the modified figure [17E] below, Toyama renders obvious *a through array contact (TAC) region* (part of 'through-memory-level via region 400') *formed between the first and second channel regions* (first and second 'memory array regions 100')." *Id.* at 85–86 (citing Ex. 1005, Fig. 17E; Ex. 1003 ¶¶ 165–166) (color emphasis omitted).



Petitioner's Modified Figure 17E depicts four copies of Figure 17E so that the structure of 17E is reproduced in both the hd1 (left-right) and hd2 (top-bottom) direction. *Id.* at 85–86. Petitioner outlines the purported "through array contact region in blue and the first and second channel regions in red. *Id.*

Petitioner's arguments as to why a POSITA would have found it obvious to implement multiple planes of Toyama's First Exemplary Structure in the hd1 (left-right) direction are not persuasive. *See* Pet. 69–77.

Patent Owner persuasively explains that that the structure shown in Figure 17E and 17F (reproduced below) includes peripheral circuitry, including driver circuitry that extends to left of the TAC region in the hd1 direction. PO Resp. 30–36; Ex. 1005, Figs. 17E, 17F; *see also* Ex. 1005 ¶¶ 49 (stating Figure 17E and 17F are top-down views of an alternative exemplary structure according to the first embodiment of the present disclosure), 251 (stating "FIGS 17E and 17F illustrate another exemplary layout of the upper level metal interconnect structures").

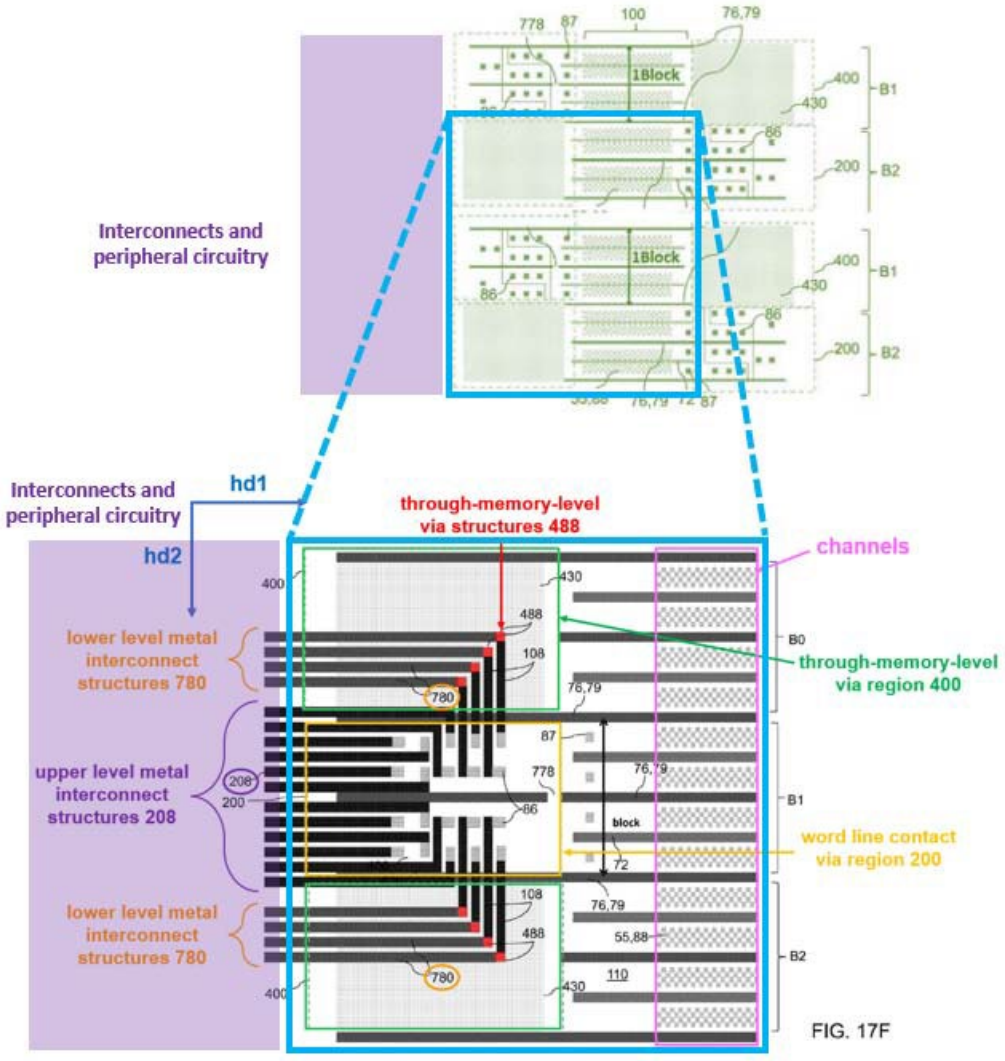


FIG. 17F

Toyama's Figures 17E and 17F, with Patent Owner's annotations, shown above, depict the driver circuits and interconnects that are located to the left

of the layout that Petitioner proposes repeating in the hd1 direction. PO Resp. 31–33. Patent Owner persuasively explains, with supporting testimony by Dr. Yang, that these regions containing the interconnects and peripheral circuitry would prevent repeating the layout in the hd1 direction because the interconnects and peripheral circuitry would be located in the same region that Petitioner proposes adding the additional memory plane. *Id.* (citing Ex. 2004 ¶ 72). Patent Owner further persuasively explains that Toyama teaches repeating the layout in the hd2 direction, not the hd1 direction, because of the location of its interconnects and peripheral circuitry, which prevents repeating the structure in the hd1 direction. *See id.* at 34 (citing Ex. 1005, Figures 17E, 17F). Patent Owner persuasively explains that Toyama Figure 17F (which is an alternate view of the structure shown in Figure 17E) shows that the memory array has interconnects and driver circuits on at least the left side, which means that in a modification adding additional planes, each plane would necessarily include these interconnects and driver circuitry on the left side. *Id.* at 35 (citing Ex. 2004 ¶ 75). We agree with Patent Owner that Petitioner has not sufficiently shown that it would have been obvious for a POSITA to repeat the structure shown in Figure 17E in the hd1 direction due to the presence of its interconnects and peripheral circuitry.

Petitioner responds that Patent Owner's argument that "a POSITA would not have made the proposed combination because Figure 17F's peripheral circuitry would interfere with another plane is not credible." Reply 17. Petitioner first asserts that Toyama's First Exemplary Structure does not require the layout of Figure 17F. *Id.* This argument is not persuasive because the Petition relies on repeating the structure shown in Figure 17E (which is an alternate view of Figure 17F) to show the modified

device meets the limitations of claim 8. *See* Pet. 66–78; *see also id.* at 68 (stating "Toyama does not expressly repeat the layout shown in Fig. 17E in the hd1 (i.e., left-right) direction. However, as explained below, a POSITA would have found it obvious to do so"), 76 (stating "Toyama does not expressly state that the layout shown in Fig. 17E, below, repeats in the hd1 (left-right) direction, but a POSITA would have been motivated to modify Toyama in this manner. That's because a POSITA would have been motivated to implement multiple planes of Toyama's first exemplary structure."); 77–78 (stating "[i]mplementing multiple planes of Toyama's first exemplary structure in the hd1 direction is shown in the modified figure [of Figure 17E] below"). Thus, the Petition's argument and evidence that it would have been obvious to a POSITA to implement multiple planes of Toyama's First Exemplary Structure is directed specifically to the embodiment of Figures 17E and 17F, not to any other embodiments of the First Exemplary Structure. *See* 37 C.F.R. § 42.104(b)(5) (stating the petition must identify the specific portions of the evidence that support the challenge).

Petitioner next argues that the placement of peripheral circuitry was well within a POSITA's skill level and further states that the four prior art references identified in the Petition depict multi-plane memory devices. Reply 18 (citing Pet. 70–76; Exs. 1014, 1023, 1024). Petitioner explains that the prior art discloses placing peripheral circuitry above and below, below, or underneath the memory array and that placing peripheral circuitry in a multi-plane device was well within the skill of a POSITA. *Id.* (citing Ex. 1043 ¶¶ 53–57). Petitioner's arguments that a POSITA could have modified and reroute circuitry in order to repeat the structure of 17E in the hd1 direction are not persuasive as they were not set forth in the Petition.

Moreover, even if a POSITA *could* have modified Toyama's Figure 17E to repeat in the hd1 direction, Petitioner has not shown that a POSITA would have done so. Although the prior art contains examples of multi-plane memory devices, Petitioner has not sufficiently shown how the existence of these multi-plane memory devices relate to modifying the *particular structure shown Toyama's Figure 17E* to repeat in the hd1 direction, given that Figure 17E already has interconnects and circuits in the hd1 direction. *See* Sur-reply 22–23. Petitioner presents only generalized assertions in its Reply that a POSITA would have been able to reroute the circuitry of Figure 17E so as to repeat the structure in the hd1 direction. *See* Reply 17–20 (stating that it was within the level of skill in the art to place peripheral circuitry in a multi-plane device but not providing sufficient evidence or argument as to how to reroute the peripheral circuitry). These generalized assertions are insufficient to show how a POSITA would have rerouted the peripheral circuitry so that Toyama's Figure 17E could repeat in the hd1 direction, or that a POSITA would have been motivated to do so. We also do not find Dr. Lee's testimony that the proposed modification is "nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance)" to be persuasive or credible. Ex. 1003 ¶ 150. We are not persuaded by this testimony because none of Petitioner's evidence persuasively shows starting with a known NAND flash device similar to that of Figure 17E and then modifying that device to implement multiple planes of that particular device. Although Petitioner has shown that there are flash devices having multiple planes, and that there are certain advantages to a flash device having multiple planes, this evidence is not sufficient to show

that a POSITA would have sought to modify the any or all flash devices to have multiple planes, let alone that it would have been obvious to modify the particular flash device depicted in Figure 17E to repeat in multiple planes. Petitioner fails to adequately discuss the characteristics of the prior art blocks that would have been modified to repeat in multiple planes sufficient to show that those characteristics apply to the structure depicted in Figure 17E.

Stated another way, evidence of flash devices having multiple planes is not sufficient to shown that it would have been obvious to modify the particular flash device of Figure 17E, which may repeat in the hd2 direction, to also repeat in the hd1 direction, so that the device would repeat in multiple planes. Other than hindsight, we do not see a persuasive reason that POSITA would have modified Toyama Figure 17E to repeat as asserted by Petitioner, particularly given the need to reroute circuitry as persuasively argued by Patent Owner.

Petitioner's arguments that a POSITA *could have* modified Figure 17E to modify the location of the peripheral circuitry because it was within a POSITA's skill level to place peripheral circuitry in a multi-plane device does not sufficiently show that a POSITA *would have been motivated* to do so. *See* Reply 17–20. Even if a POSITA *could* have modified Toyama's First Exemplary Embodiment to repeat in the left-right direction by rerouting circuitry, Petitioner has not sufficiently shown why a POISTA would have done so.

Thus, based on our review of the complete trial record, we determine that Petitioner does not establish by a preponderance of the evidence that a POSITA would have been motivated to modify Toyama's First Exemplary Structure as proposed. Consequently, we determine that Petitioner does not

establish, by a preponderance of the evidence, that independent claim 8 would have been obvious over Toyama.

(b) Claims 9, 11, and 12

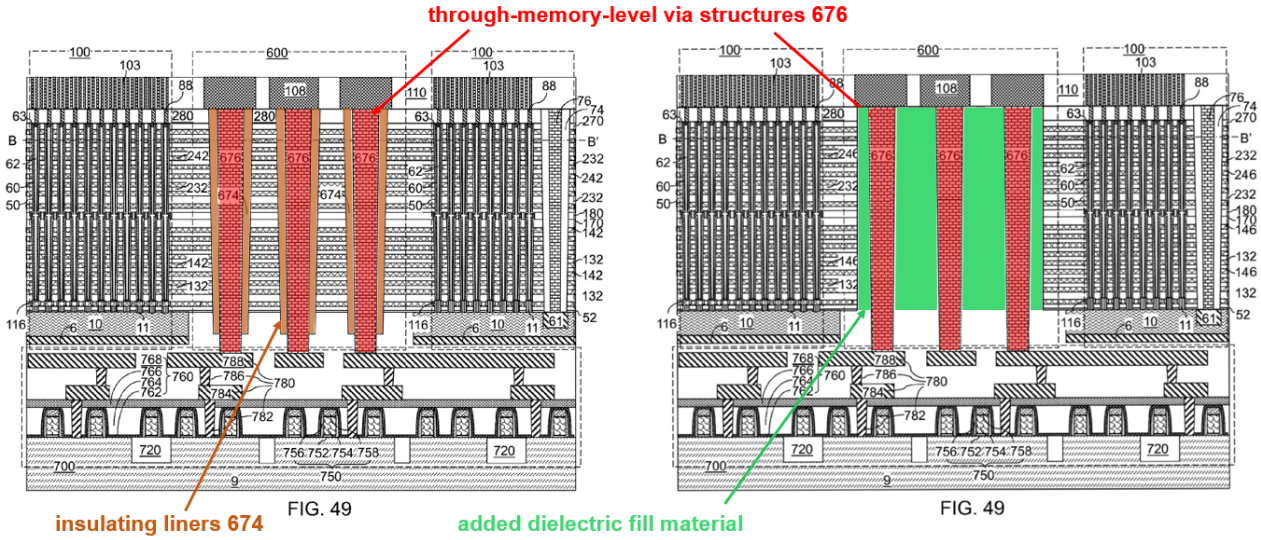
Claims 9, 11, and 12 depend, directly or indirectly, from claim 8. Ex. 1001, 24:9–11, 24:21–24. Petitioner asserts that Toyama's First Exemplary Structure teaches or suggests the limitations of these dependent claims. Pet. 94–95. None of Petitioner's arguments remedy the deficiency set forth above regarding independent claim 8. Accordingly, for the same reasons given above with respect to Petitioner's challenge of claim 8, we also conclude that Petitioner does not demonstrate by a preponderance of the evidence that claims 9, 11, or 12 would have been obvious over the teachings of Toyama.

4. Asserted Obviousness over Toyama's First Exemplary Structure in View of Toyama's Second Modification of its Fourth Exemplary Structure (Alternative Argument 3)

Petitioner argues that claims 8, 9, 11, and 12 would have been obvious over the combination of Toyama's First Exemplary Structure with Toyama's Second Modification. Pet. 96–122; Reply 21–31. Patent Owner opposes. PO Resp. 37–50; Sur-reply 24–33. In our Decision on Institution we stated that Patent Owner's arguments that Petitioner failed to address the impact of replacing the regions containing the conductive word lines, including eliminating the current that controls the memory, and invited the parties to further develop their arguments at trial. *See* Inst. Dec. 34. Upon review of the full record, we determine that Petitioner has not shown by a preponderance of the evidence that claims 8, 9, 11, or 12 would have been obvious over Petitioner's proposed combination.

(a) Claim 8

Petitioner relies on its arguments set forth above regarding Toyama's Second Modification (i.e., Petitioner's First Alternative Argument) for the preamble and claim elements [8.A], [8.C], [8.D], [8.E], and [8.F]. Pet. 108–114. For the remaining claim elements, Petitioner relies on the combination of Toyama's Second Modification and First Exemplary Structure in which a "unitary dielectric fill material" (as taught by Toyama's First Exemplary Structure) is used in place of the Second Modification's insulating liners 674. *Id.* at 98. The figures below depict Toyama's Second Modification shown in Figure 49 (left) and a modified version of Figure 49, illustrating the proposed combination. *Id.*



Toyama's original Figure 49, shown above left, with color annotations added by Patent Owner, is a cross-sectional view of Toyama's Second Modification depicting insulating liners 674 (orange) and through-level via structures 676 (red) and alternating stack (132, 142, 232, 242) of both insulating layers and electrically conductive layers. Ex. 1005 ¶¶ 103, 337, Fig. 49. Petitioner's proposed combination is shown in Modified Figure 49 (right), which depicts a block of dielectric fill material (green) and through-

level via structure 676 (red). *See* Pet. 98–99; PO Resp. 39; Ex. 1005, Fig. 49.

For claim element [8.B], Petitioner asserts that the proposed combination teaches a "dielectric structure" (the dielectric fill material) "extending vertically through the alternating conductor/dielectric layer stack" as shown in modified Figure 49, with Petitioner's color annotations added. Pet. 109–110.

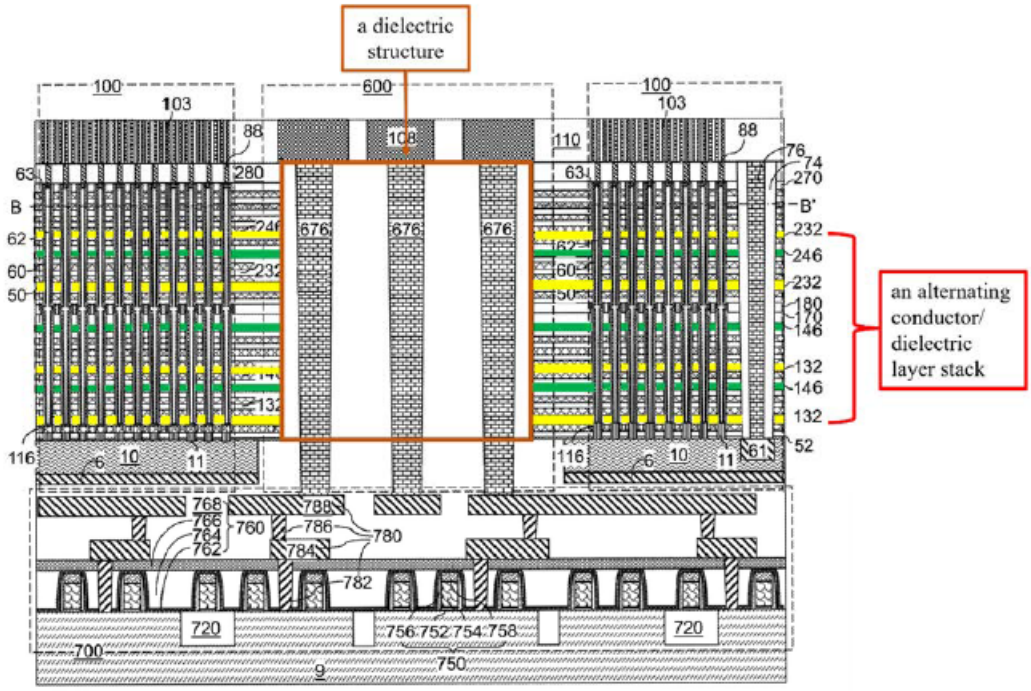


FIG. 49

Toyama's modified Figure 49, with Petitioner's annotations added, depicts Petitioner's modification of Toyama's Second Modification with the "alternating conductor/dielectric stack layer" highlighted in yellow and green and the "dielectric structure" labeled and outlined in red. Pet. 110.

For claim element [8.G], Petitioner asserts that its proposed combination teaches a "through array contact (TAC) region" (part of through-memory-level via region 600) "formed between the first and second channel regions" (first and second parts of memory array region 100)

"wherein the TAC region comprises a plurality of through array contacts (TACs)" (through-memory-level via structures 676) "extending vertically through the dielectric structure" (the unitary dielectric fill material). Pet. 114–118 (citing Ex. 1003 ¶¶ 206–208; Ex. 1005, Figs. 48B, 49)

For claim element [8.H], Petitioner assert that the proposed combination teaches a "plurality of non-electrically functional channel structures" (dummy memory stack structures 55D) "surrounding the TAC region" (part of through-memory-level via region 600) "and between the first and second channel regions" (first and second parts of memory array region 100). Pet. 119–120 (citing Ex. 1005, Fig. 48B; Ex. 1003 ¶ 209).

Petitioner asserts that a POSITA would have been motivated to modify Toyama's Second Modification to use the block of unitary dielectric fill material, instead of dielectric liners 674, to surround and electrically isolate through-memory-level via structures 676. *See* Pet. 100–101 (citing Ex. 1003 ¶ 185). Petitioner states that isolating the through-memory-level via structures is desirable to prevent electrical interference between the via structures themselves or between the via structures and other conductive elements, such as electrically conductive layers (146, 246). *Id.* at 101 (citing Ex. 1003 ¶ 185; Ex. 1005 ¶ 316).

Petitioner explains that its combination "is nothing more than the mere substitution of one element (the Second Modification's 'insulating liners 674') for another known in the field (a unitary dielectric fill material, as in the first exemplary structure's 'dielectric fill material portion 430') to yield a predictable result (e.g., electrically isolating the Second Modification's 'through-memory-level via structures')." Pet. 100 (citing Ex. 1005 ¶ 378, Figs. 16B, 48B; Ex. 1003 ¶ 183). Petitioner further asserts that a POSITA would have been motivated to use a block unitary dielectric

fill material to surround and electrically isolate via structures 676 because otherwise the via structures may electrically interfere with each other or other conductive elements, such as electrically conductive layers (146, 246). *Id.* at 100–101 (citing Ex. 1003 ¶ 185; Ex. 1005 ¶ 316). Petitioner also states that although motivation to combine does not require the combination to be superior, the combination reduces "crosstalk" or capacitive coupling between the via structures and the electrically conductive layers 146, 246 compared to Toyama's Second Modification. *Id.* at 101–103 (citing Ex. 1003 ¶¶ 185–188; Ex. 1005, Figs. 17A–B). Petitioner further states that a POSITA would have had a reasonable expectation of success to implement the combination because a POSITA would have been able to mix and match the relevant elements of Toyama's exemplary structure and Toyama teaches how to form the dielectric fill material portion 430 and the via structures within it. *Id.* at 105 (citing Ex. 1003 ¶¶ 193–194; Ex. 1005 ¶¶ 213–216, 242). Finally, Petitioner asserts that elements of the First Exemplary Structure and the Second Modification are compatible with each other because (1) outside of the "through-memory-level via region," the elements of the two structures are largely the same and (2) within the "through-memory-level via region," a POSITA would have understood that the components within the region serve a similar purpose as the both the "dielectric fill material portion 430" of the First Exemplary Structure and the insulating liners 674 of the Second Modification to electrically isolate the through array contacts from the alternating conductor/dielectric stack layer 132, 146, 232, 246. *Id.* at 106 (citing Ex. 1003 ¶ 195).

(1) Analysis

After a review of the complete record, we determine Petitioner does not show that the proposed combination would have rendered claim 8

obvious. It is Petitioner's burden to show a reason to combine. Petitioner has not done so here.

Petitioner argues that the modification is nothing more than the simple substitution of replacing the Second Modification's insulating liners 674 with the First Exemplary Structure's dielectric fill material, both of which electrically isolate via structures. *See* Pet. 100. Petitioner's argument, however, fails to address that the modification also removes other structures within the through-memory-level via region, including sacrificial layers and conductive lines, which perform multiple functions that are not performed in the proposed combination. *Compare* Toyama's (Ex. 1005) Original Fig. 49 *with* Petitioner's Modified Figure 49; *see also* PO Resp. 37–41 (citing Ex. 1005, Fig. 46A).

In particular, we are persuaded by Patent Owner's first argument that sacrificial layers 142, 242 of the Second Modification's alternating stack are used to deposit conductive material during the gate replacement process, and that the replacement of the sacrificial layers with the unitary dielectric fill material prevents this process. *See* PO Resp. 37–41 (citing, *inter alia*, Ex. 2004 ¶¶ 81–84 and explaining that the sacrificial layers 142, 242 are not present in the block of dielectric fill material in the proposed combination). We are also persuaded by Patent Owner's second argument that Petitioner's proposed modification removes large portions of the conductive layers in the array region that form word lines used to transmit signals for controlling memory and replaces them with the insulating block of dielectric fill material.[6] *Id.* at 42–46.

[6] We disagree with Petitioner's argument that Patent Owner does not dispute that the proposed combination is nothing more than a mere substitution of

Petitioner does not dispute that the Second Modification uses the sacrificial layers for gate replacement and uses the conductive layers (e.g., word lines) to transmit signals, or that the proposed combination removes both types of these layers. *See, e.g.*, Reply 21–28. Rather, Petitioner argues that a POSITA would have known how to further modify the structure of the proposed combination to achieve the functions of the removed material. *Id.* For example, with respect to the sacrificial layers used for gate replacement that are missing in the proposed combination, Petitioner asserts that a POSITA would have known how to use other structures (e.g., "backside contact trenches 79") to allow for gate replacement. *Id.* at 21–23 (citing Ex. 1043 ¶¶ 61–67). With respect to the conductive layers (e.g., word lines) used to transmit signals that are missing in the proposed combination, Petitioner asserts that a POSITA "would have known of alternative techniques for propagating the conductive layers' signals to the channel structures that are intended to receive them," such as using vias to convey electrical signals to each side of the dielectric structure. *Id.* at 24–26 (citing a modified version of Toyama Figure 48B illustrating use of modified vias).

Petitioner's arguments are not persuasive. The Petition's rationale for modifying the Toyama's Second Modification to replace liners 674 with a block of dielectric fill material, that it is a simple substitution of one known element (liners) for another (block of fill material) to obtain predictable results (insulation of vias 676), fails to account for the other elements of the

---

one element for another. Reply 28–29. Patent Owner explains that the proposed combination fails to account for elements of the Second Modification that are removed in the proposed combination. *See, e.g.*, PO Resp. 42 (stating that Petitioner's combination removes conductive word lines that are used to conduct current to control the memory and replacing them with a large insulator would eliminate that capacity in those areas).

Second Modification that were removed or the function that these removed elements performed. As such, Petitioner fails to show that its modification is a simple substitution of known elements to achieve a known result. *See* Pet. 100; *see also Arctic Cat, Inc. v. Bombadier Recreational Products, Inc.*, 876 F.3d 1350, 1363–64 (Fed. Cir. 2017)(stating that "potential hazards of the combination" indicated that the combination "would not have been a predictable solution yielding expected results."). Arguments set forth in the Reply, namely that a POSITA would have known how to further modify the Second Modification so as to perform the functions of the removed alternative stack layers and conductive layers, were not set forth in the Petition and support our determination that the Petition failed to show that the modification results in a simple substitution of one known element for another to achieve a known result.

To the extent the Petition could be read as stating that a POSITA would have modified Toyama's Second Modification to replace liners 674 with a block of dielectric fill material to "reduce capacitive coupling" or crosstalk between the via structures and electrically conductive layers (146, 246) (*see* Pet. 101–103; Ex. 1003 ¶¶ 187–188), this argument is not persuasive. Petitioner argues that "[c]apacitive coupling (also called crosstalk) is an undesirable phenomenon that causes a signal in one conductive element to affect a signal in a different conductive element where the two conductive elements are separated by an insulator." Pet. 101–102 (citing Ex. 1026, 39–40, 64, 77; Ex. 1003 ¶ 186). Petitioner asserts that "the first exemplary structure's through-memory-level via region would be less susceptible to capacitive coupling between the 'via structures' and the 'electrically conductive layers' than that of Toyama's Second Modification." *Id.* at 102–103 (citing Ex. 1003 ¶¶ 187–188). We are persuaded by Patent

Owner's argument, supported by Dr. Yang's persuasive testimony, that Toyama's Second Modification already minimizes capacitive coupling and that a POSITA would not have sought to modify the Second Modification to further reduce capacitive coupling. *See, e.g.*, PO Resp. 46–47; Ex. 2004 ¶ 92; Ex. 1005 ¶ 377. Patent Owner, with supporting testimony by Dr. Yang, persuasively explains that capacitive coupling is a function of the length or area of overlap and that, due to the fact that the electrically conductive layers run perpendicular to the via structures, and the presence of the insulating liners, the length or area of the proximity of the via structures and the electrically conducive layers is *de minimus*. PO Resp. 46–47; Ex. 1026, 64; Ex. 1005, Fig. 49; Ex. 2004 ¶ 92. As such, capacitive coupling is already minimized and no further reduction is required. *See* PO Resp. 47; Ex. 2004 ¶ 92.

Petitioner's argument set forth in its Reply as to why a POSITA would have sought to minimize capacitive coupling is not persuasive. *See* Reply 28–31; Ex. 1043 ¶¶ 80–83. Toyama expressly states that the structures used in the Second Modification "minimize signal loss and capacitive coupling." Ex. 1005 ¶ 377. Dr. Lee's testimony that this language in Toyama shows capacitive coupling is a "significant concern" is not persuasive. *See* Ex. 1043 ¶¶ 81–82.

Petitioner replies that even if Patent Owner's contention is true (i.e., that Toyama's Second Modification already minimizes crosstalk), that all Petitioner has to do is show that the proposed combination is a "suitable option." Reply 29–31. We disagree because, as noted above, Petitioner has not sufficiently shown that replacing the dielectric liners *and the various layers* of Toyama's Second Modification with a block of dielectric material is a simple substitution of one known element for another.

Thus, for the foregoing reasons, Petitioner has not sufficiently shown that a POSITA would have been motivated to replace dielectric liners 674 and the various layers with a block of dielectric material. As such, Petitioner has not shown by a preponderance of the evidence that claim 8 would have been obvious over the combination to Toyama's Second Modification and its First Exemplary Structure.

(b) Claims 9, 11, and 12

Claims 9, 11, and 12 depend, directly or indirectly, from claim 8. Ex. 1001, 24:9–11, 24:21–24. Petitioner asserts that Toyama's Second Modification in combination with its First Exemplary Structure also teaches or suggests the limitations of these dependent claims. None of Petitioner's arguments remedy the deficiency set forth above regarding independent claim 8. Accordingly, for the same reasons given above with respect to Petitioner's challenge of claim 8, we also conclude that Petitioner does not demonstrate by a preponderance of the evidence that claims 9, 11, or 12 would have been obvious over the teachings of Toyama.

III. CONCLUSION

After reviewing the record and weighing the evidence offered by both parties, we determine that Petitioner fails to show, by a preponderance of the evidence, that claims 8, 9, 11, or 12 of the '806 patent are unpatentable.

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
8, 9, 11, 12	103	Toyama		8, 9, 11, 12

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not established by a preponderance of the evidence that claims 8, 9, 11, and 12 of the '806 patent are unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

For PETITIONER:

Jeremy Jason Lang
Travis Jensen
K. Patrick Herman
Jared Bobrow
Parth Sagdeo
ORRICK, HERRINGTON & SUTCLIFFE LLP
jlang@orrick.com
tjensen@orrick.com
pherman@orrick.com
jbobrow@orrick.com
psagdeo@orrick.com

For PATENT OWNER:

James L. Davis, Jr.
Andrew T. Radsch
Christopher M. Bonny
ROPES & GRAY LLP
james.l.davis@ropesgray.com
andrew.radsch@ropesgray.com
christopher.bonny@ropesgray.com