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Paper 17
Date: May 15, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2025-00002
Patent 11,880,319 B2

Before NORMAN H. BEAMER, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

BEAMER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1–20 of U.S. Patent No. 11,880,319 B2, issued on July 12, 2022 (Ex. 1001, "the '319 patent). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp."). With our authorization, Petitioner filed a Preliminary Reply (Paper 11, "Prelim. Reply") and Patent Owner filed a Preliminary Sur-reply (Paper 12, "Prelim. Sur-reply").

Institution of an *inter partes* review is authorized when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Based on the current record, and for the reasons explained below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one challenged claim, and we institute an *inter partes* review.

II. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. as real parties-in-interest. Pet. 1. Patent Owner identifies itself as the real party-in-interest. Paper 4, 1 (Patent Owner's Mandatory Notices).

B. Related Matters

The parties identify the following pending related matters:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, IPR2025-00001 (U.S. Patent No. 11,386,024);
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*,

No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021) (U.S. Patent Nos. 9,858,218 and 10,474,595);
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:23-cv-01122-RGA (D. Del. filed Oct. 9, 2023) (U.S. Patent No. 11,386,024);
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:24-cv-00614 (D. Del. filed May 22, 2024) (U.S. Patent No. 11,880,319); and
- U.S. Application No. 18/413,017.

Pet. 1; Paper 4, 1–2. The parties also identify the following concluded related matters:

- *Netlist, Inc. v. SK hynix Inc., et al.*, Nos. 8:16-cv-01605 (C.D. Cal. filed Aug. 31, 2016) (U.S. Patent No. 8,489,837);
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016) (U.S. Patent No. 8,489,837);
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00548 (U.S. Patent No. 8,489,837);
- *Netlist, Inc. v. SK hynix Inc. et al.*, No. 8:17-cv-01030 (C.D. Cal. filed June 14, 2017) (U.S. Patent No. 9,535,623) ("the '623 patent");
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017) (U.S. Patent No. 9,535,623);
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00303 (U.S. Patent No. 9,535,623);
- *Netlist, Inc. v. SK hynix Inc. et al.*, No. 6:20-cv-00194 (W.D. Tex. filed Mar. 17, 2020) (U.S. Patent Nos. 9,858,218 and 10,474,595);
- *SK hynix Inc., et al. v. Netlist, Inc.*, IPR2020-01042 (U.S. Patent No. 10,474,595);
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2020-01044 (U.S. Patent No. 9,858,218);
- *Samsung Electronics Co., Ltd. v Netlist, Inc.*,

IPR2022-00062 (U.S. Patent No. 9,858,218); and
- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2022-00064 (U.S. Patent No. 10,474,595).

Pet. 1–3; Paper 4, 2.

C. The '319 Patent

The '319 patent is titled "Memory Module Having an Open-Drain Output For Error Reporting And For Initialization," and generally relates to "handshaking with a memory module during or upon completion of initialization." Ex. 1001, code (54), 1:26–27. The '319 patent explains that memory subsystems, "such as memory modules[,] are generally involved in the initialization procedure for computer systems." *Id.* at 1:31–33. For example, "the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization." *Id.* at 1:38–40. However, the '319 patent states that there is no existing method of handshaking between the system memory controller and the memory module during initialization. *Id.* at 2:65–3:1. As a result, the system memory controller "does not monitor the error-out signal from the [memory module]" and therefore, "perform[s] blind execution." *Id.* at 3:1–4. According to the '319 patent, this has not been a serious issue because the system memory controller "generally has complete control over the initialization procedure." *Id.* at 3:7–9. However, certain configurations have the system memory controller "handing over the one or more parts of the initialization operation sequence to the memory subsystem." *Id.* at 3:11–12. In these types of configurations, the system memory controller may insert a waiting period of predetermined length during which it is idle while the memory subsystem controller undergoes initialization. *Id.*

at 3:17–20. However, this approach has shortcomings in that the time for the memory subsystem controller to complete the task may vary and may be longer or shorter than the predetermined period of time that the system memory controller is idle. *Id.* at 3:20–33.

The '319 patent describes two methods of handshaking between a system memory controller and a memory module: notifying and polling. Ex. 1001, 3:43–44. In polling, the system memory controller "reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation." *Id.* at 3:45–47. The '319 patent explains that polling is "generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation." *Id.* at 3:50–53. Therefore, the notifying method, where the memory subsystem controller sends a signal to the system memory controller when it completes the required or requested operation, is described by the '319 patent as advantageous because it allows the system memory controller to execute one or more independent commands while it waits for the notification signal from the memory subsystem controller. *Id.* at 3:64–4:5.

The embodiments described in the '319 patent provide "a method of establishing a handshake mechanism based on notification signaling." Ex. 1001, 4:6–8. "In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the [system memory controller] and the memory subsystem controller [which] can be an open drain signaling from the memory subsystem controller to the [system memory controller]." *Id.* at 4:8–16.

The '319 Patent describes a memory module coupled to a system memory controller of a host computer system via an interface that includes data, address and control signal pins and an output pin. Ex. 1001, 1:44–48, 4:26–29. The memory module operates in two modes, an operational mode to perform normal memory read/write, pre-charge, and refresh operations, and an initialization mode to receive and execute training or initialization sequences to prepare the memory module for normal read/write operation. *Id.* at 4:29–33, 6:2–7, 6:45–56. The memory module has an open-drain output pin which it uses to indicate a parity error in the first mode for normal read/write operations. *Id.* at 8:26–31. In the second mode of operation, the memory module uses the same output pin to notify the memory controller of the status of its execution of the training sequence, i.e., whether execution of the training sequence is in progress or has been completed. *Id.* at 8:31–38.

Figure 2 of the '319 Patent, reproduced below, illustrates an embodiment with multiple memory modules performing handshaking with a memory controller. Ex. 1001, 2:38–42.

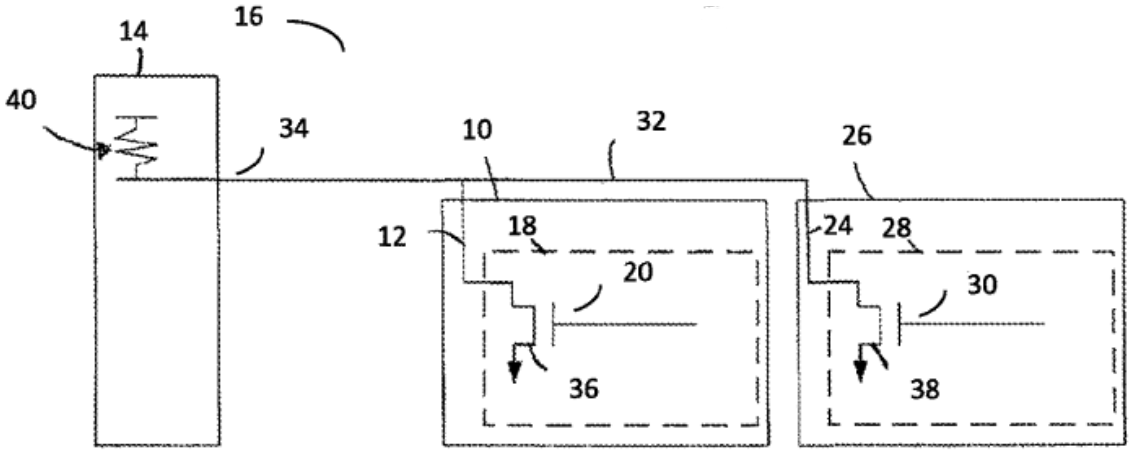

Figure 2

Specifically, Figure 2 shows host computing system 16 including system memory controller 14 connected to first and second memory modules 10, 26. *Id.* at 4:24–25, 6:15–19, 9:47–48. The memory modules 10, 26 include respective controller circuits 18, 28 with notification circuits 20, 30. *Id.* at 4:33–34, 4:36–38, 9:16–19. Notification circuits 20, 30 have corresponding transistors 36, 38 with open-drain configurations. *Id.* at 9:49–52. As memory modules 10, 26 carry out their training or initialization sequences, memory modules 10, 26 drive the gates of the transistors 36, 38 high, which pulls their outputs 12, 24 low, signaling to the memory controller 14 via input 34 that the initialization sequences have not been completed. *Id.* at 9:59–10:24. As each memory module 10, 26 completes its initialization sequence, the module drives the gate of its respective transistor 36 or 38 low, causing its output 12 or 24 to enter a high-impedance state. *Id.* When all modules' transistor outputs are in high-impedance states, input 34 draws high, notifying the system memory controller 14 that all memory modules have completed their initialization sequences and are ready for normal read/write operation. *Id.*

The memory module may comprise a printed-circuit board (PCB) with dynamic random-access memory (DRAM) elements and a module controller. Ex. 1001, 4:43–44, 5:21–23. The PCB may have an interface with edge connections for data, address and control, and error signals (including parity and notification signals). *Id.* at 5:10–20, 8:23–33. The module controller may be an integrated circuit mounted on the PCB. *Id.* at 7:58–62.

Another memory module configuration is shown in Figure 3, reproduced below.

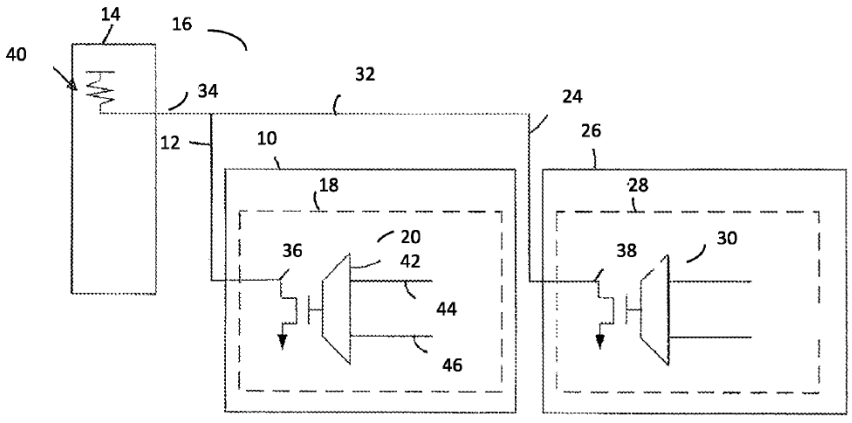

Figure 3

Figure 3 illustrates an additional embodiment with multiple memory modules performing handshaking with a system memory controller. Ex. 1001, 2:43–48, 11:15–19. Figure 3 adds multiplexors 42 to Figure 2 connected to the transistor gates to provide either a parity error signal 46 when the memory module is in operational mode or a task in progress signal 44 when the memory module is in initialization mode or executing at least one initialization sequence, or a "signal related to one or more training sequences" (the notification signal). *Id.* at code (57), 11:18–29. Thus, "the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode." *Id.* at 11:29–34.

D. Illustrative Claims

Claims 1 and 11 are independent. Ex. 1001, 14:41–15:4, 15:61–16:23. Independent claim 1 is representative and is reproduced below, with Petitioner's identifiers in bolded brackets.

1. **[1.a]** A memory subsystem operable with a system memory controller of a host system, comprising:

[1.b.1] dynamic random access memory elements on a printed circuit board and **[1.b.2]** configurable to communicate data signals with the system memory controller; and

[1.c.1] a memory subsystem controller on the printed circuit board and [**1.c.2]** coupled to the dynamic random access memory elements, **[1.c.3]** the memory subsystem controller having an open drain output, **[1.d.1]** wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and **[1.d.2]** a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations;

[1.e.1] wherein, during the normal memory read or write operations, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and **[1.e.2]** the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the normal memory read or write operations; and

[1.e.3] wherein, during the initialization operation, the memory subsystem controller is configured to output via the open drain output a signal related to one or more parts of the initialization operation sequences.

Id. at 14:41–15:4. Claim 11 is a method claim reciting similar limitations.

Id. at 15:61–16:23.

E. Evidence

Petitioner relies on the following references, as well as, *inter alia*, the Declaration of Dr. Donald Alpert (Ex. 1003).

Name	Patent Document	Exhibit
Hazelzet	U.S. Patent Pub. No. 2008/0098277 A1 to Hazelzet, published Apr. 24, 2008	1014
JEDEC	JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR Memory Initialization Chapter Proposal (Dec. 2009)	1015
Buchmann	U.S. Patent No. 8,139,430 B2 to Buchmann et al., issued Mar. 20, 2012	1016
Wang	U.S. Patent No. 8,386,722 B1 to Wang et al., issued Feb. 26, 2013	1090
Kim	U.S. Patent No. 8,359,521 B2 to Kim et al., issued Jan. 22, 2013	1017

F. Asserted Grounds

Petitioner asserts that claims 1–20 would have been unpatentable on the following grounds (Pet. 4):

Claim(s) Challenged	35 U.S.C. §[1]	Reference(s)/Basis
1–20	103(a)	Hazelzet, JEDEC
1–20	103(a)	Hazelzet, Buchmann
1–20	103(a)	Hazelzet, Wang
1–20	103(a)	Hazelzet, JEDEC, Kim
1–20	103(a)	Hazelzet, Buchmann, Kim
1–20	103(a)	Hazelzet, Wang, Kim

[1] Because the '319 patent issued from a patent application that was filed before March 16, 2013, patentability is governed by the version of 35 U.S.C. § 103 preceding the Leahy-Smith America Invents Act ("AIA"), Pub L. No. 112–29, 125 Stat. 284 (2011).

III. PRELIMINARY MATTERS

A. Background and Prior Proceedings

The '319 patent was filed as U.S. Patent Application 17/840,593 on June 14, 2022, and is a continuation of U.S. Patent Application 16/680,060 filed on November 11, 2019, now U.S. Patent No. 11,386,024 ("the '024 patent"), which is a continuation of U.S. Patent Application 15/857,553, filed on December 28, 2017, now U.S. Patent No. 10,474,595 ("the '595 patent"), which is a continuation of U.S. Patent Application 15/088,115, filed on April 1, 2016, now U.S. Patent No. 9,858,218 ("the '218 patent"), which is a continuation of U.S. Patent Application 13/942,721, filed on July 16, 2013, now U.S. Patent No. 9,311,116 ("the '116 patent"), which is a continuation of U.S. Patent Application 12/815,339, filed on June 14, 2010, now U.S. Patent No. 8,489,837 ("the '837 patent"), which claims priority to provisional application No. 61/186,799, filed June 12, 2009. Ex. 1001, codes (21), (22), (60), (63). The '623 patent is a continuation of the '116 patent, which is a continuation of the '837 patent. Ex. 1031, code (63).

In IPR2022-00062, the Board determined that claims 1–22 of the '218 patent were obvious over the combination of Hazelzet and Buchmann, and that claims 3–6, 10–12, and 17–20 were obvious over the combination of Hazelzet, Buchmann, and Kim. Ex. 1102. In IPR2022-00064, the Board determined that claims 1–24 of the '595 patent were obvious over the combination of Hazelzet and Buchmann, and that claims 3–7, 12–14, 20, 22, and 23 were obvious over the combination of Hazelzet, Buchmann, and Kim. Ex. 1103. Similarly, in IPR2018-00303, the Board determined, among other things, that claims 1–29 of the '623 patent were obvious over the combination of Hazelzet and Buchmann, and that claims 10, 15, and 27

were obvious over the combination of Hazelzet, Buchmann, and Kim. Ex. 1034. Here, Petitioner challenges claims 1–20 of the '319 patent over Hazelzet and Buchmann, as well as Hazelzet, Buchmann, and Kim. Pet. 4.

B. Discretionary Denial under 35 U.S.C. 325(d)

Patent Owner contends that the Board should deny institution under 35 U.S.C. § 325(d). Prelim. Resp. 10–22. We decline to exercise discretion to deny institution under § 325(d) for the reasons discussed below.

1. Applicable Framework

35 U.S.C. § 325(d) provides that, in determining whether to institute an *inter partes* review, "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." The Board uses a two-part framework when determining whether to exercise its discretion under 35 U.S.C. § 325(d), specifically: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if so, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*").

In applying the two-part framework, we consider a number of non-exclusive factors in evaluating whether to exercise its discretion under § 325(d). *See Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5,

first para.) ("*Becton, Dickinson*"); *see also Advanced Bionics* at 9–11. The factors set forth in *Becton, Dickinson* are as follows:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which petitioner relies on the prior art or patent owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, Paper 8 at 17–18. *Becton, Dickinson* factors (a), (b), and (d) relate to whether the art or arguments presented in the Petition are the same or substantially the same as those previously presented to the Office. *Advanced Bionics*, Paper 6 at 10. The art or arguments presented in the Petition are not "substantially the same" as those previously presented to the Office when there are differences between them that are material to the Office's prior consideration of the art and arguments. *Wolfspeed, Inc. v. Trs. of Purdue Univ.*, IPR2022-00761, Paper 13 at 7–8 (PTAB (Vidal) Mar. 30, 2023).

Factors (c), (e), and (f) "relate to whether the petitioner has demonstrated a material error by the Office" in its prior consideration of that art or arguments. *Advanced Bionics*, Paper 6 at 10. Only if the same or substantially the same art or arguments were previously presented to the Office do we consider whether petitioner has demonstrated a material error by the Office. *Id.* "At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown." *Id.* at 9.

2. Whether the Same or Substantially the Same Art or Arguments Were Previously Presented to the Office

Patent Owner contends that, with the exception of Wang, each of Hazelzet, the JEDEC reference, Buchmann, and Kim were cited to and considered by the Examiner during prosecution of the '319 patent. Prelim. Resp. 14–16. Patent Owner argues that Hazelzet was applied by the Examiner in a non-final Office Action, and by the same Examiner in two Office Actions in parent application 16/680,060 ("the '060 application"). *Id.* at 14 (citing Ex. 1002, 60–67; Ex. 1112, 190–198, 298–310). Patent Owner further argues that the JEDEC reference, Buchmann, and Kim were cited in an IDS. *Id.* at 15–16 (citing Ex. 1002, 223, 230). In addition, Patent Owner argues that the Examiner considered Petitioner's prior petitions, and Final Written Decisions, from IPR2022-00062 and IPR2022-00064, which asserted Hazelzet in combination with Buchmann, the draft JEDEC proposal, and/or Kim against the claims of related U.S. patents 9,858,218 and 10,474,595. *Id.* at 16 (citing Ex. 1002, 222, 230; Ex. 1098; Ex. 1100).

Patent Owner also argues that the grounds that Petitioner relies on present a theory of patentability that was already considered by the

Examiner and overcome during prosecution. Prelim. Resp. 17–20. In particular, argues Patent Owner, the Examiner considered and found not obvious the theory of adding buffering and training sequences to Hazelzet in light of a JEDEC document ("JESD206") different from the JEDEC reference relied on here. *Id.* (citing Ex. 1002, 65–66; Ex. 1025).

There is no dispute that Hazelzet, the JEDEC reference, Buchmann, and Kim were before the Examiner during prosecution of the '319 patent, and that Hazelzet was applied in Office Actions. Although Petitioner is correct that the Examiner did not consider the combinations as proposed by Petitioner—Hazelzet and the JEDEC reference; Hazelzet and Buchmann; and Hazelzet and Kim—we find this sufficient to move on to the second question under *Advanced Bionics*.

3. Whether Petitioner has Demonstrated that the Office Erred in a Manner Material to the Patentability of the Challenged Claims

Petitioner argues that the Examiner did not consider or analyze the combinations of art presented in the Petition, nor did the applicant offer any analysis of the claims in view of the Board's final written decisions in IPR2018-00303, IPR2022-00062, and IPR2022-00064, which invalidated substantially similar claims in the '623, '218, and '595 patents over the combination of Hazelzet and Buchmann and Hazelzet, Buchmann, and Kim. Pet. 115–116; Prelim. Reply 1–3. Petitioner argues that these three final written decisions demonstrate that the Examiner materially erred in allowing the claims. *Id.* Patent Owner argues that Petitioner has not carried its burden of demonstrating material error, because the claims of the '319 patent are patentably distinct from the '623, '218, and '595 patents, and

Petitioner merely points to the Board's final written decisions in these three proceedings. Prelim. Resp. 20–21.

Becton Dickinson factors (c), (e), and (f) weigh against exercising our discretion under § 325(d). Based on the current record, we agree with Petitioner that the claims of the '319 patent are substantially similar to the invalidated claims in the '623, '218, and '595 patents.[2] *Compare* Ex. 1001, 14:41–17:12 ('319 patent), with Ex. 1031, 15:26–18:54 ('623 patent); Ex. 1095, 14:38–17:12 ('218 patent); Ex. 1097, 14:39–19:7 ('595 patent); *see also* Pet. xvii–xli (reproducing claims of the '319, '623, '218, and '595 patents). Under factor (c), Petitioner shows that the Examiner's previous consideration of Hazelzet, Buchmann, and Kim was insufficient. For example, although Hazelzet was applied, it was not applied in combination with Buchmann and/or Kim, and there was no statement by the Examiner explaining why the claims of the '319 patent were deemed allowable over these references. *See* Ex. 1002. We also find that Petitioner shows that factors (e) and (f) are met in light of the final written decisions in IPR2018-00303, IPR2022-00062, and IPR2022-00064, which demonstrate how the Examiner erred in its evaluation of the asserted prior art, and that the combinations of Hazelzet, Buchmann and Hazelzet, Buchmann, and Kim warrant reconsideration.

Thus, *Becton Dickinson* factors (c), (e), and (f) show that the Office erred in a manner material to the patentability of the challenged claims. *Advanced Bionics*, Paper 6 at 8. Accordingly, we decline to exercise our discretion to deny institution under § 325(d).

[2] We discuss this further in Section III.D below in connection with Petitioner's collateral estoppel arguments.

C. Considerations Under 35 U.S.C. § 314

Patent Owner argues that we should exercise our discretion to deny institution under *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 at 42 (PTAB Jan. 24, 2019) (informative) and *Chevron Oronite Co. LLC. v. Infineum USA L.P.*, IPR2018-00923, Paper 9 at 10–11 (PTAB Nov. 7, 2018) (informative). Prelim. Resp. 55–57. When deciding whether to exercise our discretion, we may consider the number of claims and grounds that meet the reasonable likelihood standard and whether, in the interests of efficient administration of the Office and integrity of the patent system, the entire petition should be denied. *Deeper*, Paper 7 at 42; *Chevron*, Paper 9 at 10–11. Here, Petitioner demonstrates a reasonable likelihood of prevailing on its challenges involving Hazelzet and Buchmann, and Hazelzet, Buchmann and Kim, which address all challenged claims. On this record, and based on the particular facts of this proceeding, we find that instituting a trial is an efficient use of the Board's time and resources.

D. Collateral Estoppel

Petitioner contends that estoppel precludes Patent Owner from relitigating "virtually every issue presented by this Petition" because the Board previously invalidated substantially similar claims in related patents, applying the same art as in Grounds 2 (Hazelzet, Buchmann) and 5 (Hazelzet, Buchmann, Kim) presented here. Pet. 5 (referring to IPR2018-00303 (the '623 patent), IPR2022-00062 (the '218 patent), and IPR2022-00064 (the '595 patent)). Petitioner states that all of the claims challenged in these prior *inter partes* review proceedings have been cancelled by IPR Certificates. *Id.* (citing Ex. 1031, 16; Ex. 1095, 16; Ex. 1097, 19). Petitioner further contends that each of the claims of the '319

patent are substantially identical to claims of the '623, '218, and '595 patents that the Board found obvious over Hazelzet and Buchmann and Hazelzet, Buchman, and Kim, that such issues were actually litigated and essential to the final written decisions in those proceedings, and that Patent Owner had full and fair opportunities to litigate all the issues before the Board in each of the three proceedings. *Id.* at 6–7.

Patent Owner contends that Petitioner has failed to show that any of the factors to invoke collateral estoppel are satisfied. Prelim. Resp. 7. Patent Owner argues that Petitioner has not shown that the challenged claims have "materially the same scope" as the claims of the related patents. *Id.* at 7–8. Specifically, Patent Owner argues that Petition has provided no analysis or comparison in scope of any of the relevant claims in the Petition, and simply incorporates by reference "large swaths of Dr. Alpert's declaration, prior Board decisions, and other record evidence." *Id.* at 8. Patent Owner also argues that the claims of the '319 patent are materially different than those of the related patents, pointing out that the '319 claims recite first and second distinct signaling interfaces, absent from the related patents. *Id.* at 8–9. And Patent Owner further points out that an obviousness-type double patenting rejection over claims of the '595 patent was resolved by adding these signaling interface requirements. *Id.* at 9 (citing Ex. 1002, 63, 97, 103, 120, 210). In addition, Patent Owner argues that Petitioner has only presented conclusory allegations for the remaining factors. *Id.* at 10.

"It is well established that collateral estoppel applies to IPR proceedings." *Google LLC v. Hammond Dev. Int'l*, 54 F.4th 1377, 1381 (Fed. Cir. 2022). Collateral estoppel, i.e., issue preclusion, applies when

"(1) a prior action presents an identical issue; (2) the prior action actually litigated and adjudged that issue; (3) the judgment in that prior action necessarily required determination of the identical issue; and (4) the prior action featured full representation of the estopped party." *VirnetX Inc. v. Apple Inc.*, 909 F.3d 1375, 1377 (Fed. Cir. 2018) (quoting *Stephen Slesinger, Inc. v. Disney Enters., Inc.*, 702 F.3d 640, 644 (Fed. Cir. 2012)). This preclusive effect also applies to "related claims that present identical issues of patentability." *MaxLinear, Inc. v. CF CRESPE LLC*, 880 F.3d 1373, 1377 (Fed. Cir. 2018); *Google*, 54 F.4th at 1381 ("[C]ollateral estoppel may apply even if the patent claims use slightly different language to describe substantially the same invention.") (internal quotation marks omitted); *Ohio Willow Wood Co. v. Alps S., LLC*, 735 F.3d 1333, 1342 (Fed. Cir. 2013) ("Our precedent does not limit collateral estoppel to patent claims that are identical.").

As described above, the '319 patent is a continuation of the '024 patent, which is a continuation of the '595 patent that was challenged in IPR2022-00064, which is a continuation of the '218 patent that was challenged in IPR2022-00062, which is a continuation of the '116 patent, which is a continuation of the '837 patent. Ex. 1001, code (63). Similarly, the '623 patent that was challenged in IPR2018-00303 is a continuation of the '116 patent, which is a continuation of the '837 patent. Ex. 1031, code (63).

In IPR2022-00062, the Board determined that claims 1–22 of the '218 patent were obvious over the combination of Hazelzet and Buchmann, and that claims 3–6, 10–12, and 17–20 were obvious over the combination of Hazelzet, Buchmann, and Kim. Ex. 1102. In IPR2022-00064, the Board

determined that claims 1–24 of the '595 patent were obvious over the combination of Hazelzet and Buchmann, and that claims 3–7, 12–14, 20, 22, and 23 were obvious over the combination of Hazelzet, Buchmann, and Kim. Ex. 1103. Although Patent Owner appealed these two final written decisions, the parties later jointly stipulated to voluntarily dismiss the appeals, and the appeals have been dismissed. Ex. 1104. These two decisions, therefore, became final. *See Papst Licensing GmbH & Co. KG v. Samsung Elects. Am., Inc. et al.*, 924 F.3d 1243, 1249 (Fed. Cir. 2019). Similarly, in IPR2018-00303, the Board determined, among other things, that claims 1–29 of the '623 patent were obvious over the combination of Hazelzet and Buchmann, and that claims 10, 15, and 27 were obvious over the combination of Hazelzet, Buchmann, and Kim. Ex. 1034. Here, Petitioner challenges claims 1–20 of the '319 patent over Hazelzet and Buchmann, as well as Hazelzet, Buchmann, and Kim. Pet. 4.

Petitioner provides a chart of the challenged claims in the '319 patent, and separate charts of the invalidated claims in the '623, '595, and '218 patents. Pet. xvii–xli. Further, in the analysis of each of claims 1–20 of the '319 patent, Petitioner provides citations to the corresponding analysis for the Hazelzet/Buchmann and Hazelzet/Buchmann/Kim combinations from the final written decisions in IPR2018-00303, IPR2022-00062, and IPR2022-00064 for the corresponding claims and claim limitations in the '623, '218 and '595 patents. *See id.* at 50–110. For example, Petitioner contends that limitation [1.e.2] of the '319 patent is equivalent to limitation [1.b] and claims 2, 7, and 9 of the '623 patent, limitations [1.f], [1.h], and claim 5 of the '218 patent, limitations [1.e.ii] and [1.f.iii] and claim 5 of the '595 patent. *Id.* at 78 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex.

1102, 47–52, 64–66; Ex. 1103, 46–47, 50, 69–71). Petitioner identifies similar equivalencies for each of the dependent claims and additional independent claims, as well as Petitioner's motivation to combine the references. *Id.* at 40–50, 81–110. Given this showing by Petitioner, we disagree with Patent Owner that Petitioner has not sufficiently shown that the challenged claims have "materially the same scope" as the claims of the related patents.

The present record supports that the asserted claims of the '319 patent are substantially similar to the invalidated claims of the '623, '595 and '218 patents. Pet. xvii–xli; *id.* at 55–112. For example, comparing claim 1 of the '319 and '595 patents, the patents recite comparable requirements, including:

> "[a] memory subsystem operable with a system memory controller of a host system" ('319 patent), and "[a] memory module operable with a memory controller of a host system" ('595 patent);
>
> "dynamic random access memory elements on a printed circuit board" ('319 patent), and "dynamic random access memory elements on the printed circuit board" ('595 patent);
>
> "a memory subsystem controller on the printed circuit board and coupled to the dynamic random access memory elements, the memory subsystem controller having an open drain output" ('319 patent), and "a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output" ('595 patent);
>
> "during the normal memory read or write operations, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals"

> ('319 patent), and "wherein the module controller is configurable to receive . . . the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller . . . in accordance with the address and control signals" ('595 patent);
>
> "the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the normal memory read or write operations" ('319 patent), and "the module controller is further configurable to output via the open drain output . . . a signal indicating a parity error" ('595 patent);
>
> "during the initialization operation, the memory subsystem controller is configured to output via the open drain output a signal related to one or more parts of the initialization operation sequences" ('319 patent) and "the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output" ('595 patent);

Pet. xvii, xxxiii–xxxiv.

Additional limitations in claim 1 of each patent further recite configuration of the memory subsystem controller ('319 patent)/module controller ('595 patent) to perform operations relating to initialization ('319 patent)/training sequences ('595 patent) or for normal memory read or write operations (both patents). *Id.* The same is true when comparing the dependent claims, for example, comparing claim 2 of the '319 patent with claims 3 and 7–9 of the '623 patent, claims 3–5 of the '218 patent, and claims 3–5 and 7 of the '595 patent. *Id.* at xvii–xviii, xxiii, xxix, xxxiv–xxxv. Although the claim language is not identical, it need not be to invoke collateral estoppel. *See Ohio Willow Wood,* 735 F.3d at 1342 (stating that collateral estoppel is not limited "to patent claims that are identical . . . If the

differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity, collateral estoppel applies.").

Although, as Patent Owner argues, during the prosecution of the '319 patent, an obviousness-type double patenting rejection over claims of the '595 patent was resolved by adding the requirement of distinct first and second distinct signaling interfaces (Prelim. Resp. 8–9), Petitioner correctly responds that the amended claim language required the same "open drain output" for both signaling interfaces, which is a materially identical requirement of the '595, as well as the '218 and '623, claims. Prelim. Reply 1–2. In sum, the differences between the claims in the '319 patent and the '623, '218, and '525 patents do not appear to materially alter the question of invalidity.

We therefore find, on this record, that Petitioner has established that prior actions, i.e., IPR2018-00303, IPR2022-00062, IPR2022-00064, presents an identical issue, i.e., obviousness over Hazelzet and Buchmann or obviousness over Hazelzet, Buchmann, and Kim. For the remaining three factors, each of the proceedings actually litigated and adjudged that issue in the final written decision, the judgment necessarily required determination of that issue, and there is no evidence in the record that Patent Owner was not fully represented in any of the three proceedings. Therefore, on this record, we are preliminarily persuaded that Patent Owner is collaterally estopped as to the challenges involved in the Petition, i.e., obviousness of claims 1–20 of the '319 patent.

However, to the extent that this case is not resolved on the grounds of collateral estoppel, as discussed below, we determine that Petitioner has

established a reasonable likelihood that it would prevail with respect to at least one challenged claim to the asserted grounds of patentability over Hazelzet and Buchmann, or Hazelzet, Buchmann, and Kim.

E. Priority Date of the '319 Patent Claims

Petitioner contends that the JEDEC reference is prior art because the claims of the '319 patent are not entitled to the provisional application priority date because Patent Owner cannot show written description support for multiple claim limitations. Pet. 7–10. That is, Petitioner contends that the effective filing date of the '319 patent is no earlier than June 14, 2010. *Id.*

At this stage, Patent Owner does not challenge Petitioner's contentions as to the priority date of the '319 patent. *See, e.g.*, Prelim. Resp. 33, 54 (arguing that Petitioner has not demonstrated that the JEDEC reference was publicly accessible before the critical date, either June 2009 or June 2010). This issue only affects the challenges involving the JEDEC reference. As discussed below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one challenged claim in the challenges involving Hazelzet and Buchmann and Hazelzet, Buchmann, and Kim. Accordingly, for purposes of this Decision, we need not address the appropriate effective filing date of the '319 patent.

F. Patent Owner's Incorporation by Reference Arguments

Patent Owner argues that the Petition's "excessive use of incorporation by reference violates the Board's Rules and fails to provide Patent Owner and the Board with adequate notice of Petitioner's patentability challenges." Prelim. Resp. 4. Specifically, Patent Owner argues that "[t]he Petition widely and impermissibly incorporates by

reference from other documents–such as Dr. Alpert's declaration, prior Board decisions, and other evidence in the record — often presenting conclusory statements followed by length and unexplained string citations." *Id.* at 5.

The applicable rules provide that "[a]rguments must not be incorporated by reference from one document into another document." 37 C.F.R. § 42.6(a)(3). As explained by the Federal Circuit:

> When promulgating § 42.6(a)(3), the Patent and Trademark Office explained that the rule "minimizes the chance that an argument would be overlooked and eliminates abuses that arise from incorporation and combination," Rules of Practice for Trials Before the Patent Trial and Appeal Board and Judicial Review of Patent Trial and Appeal Board Decisions, 77 Fed. Reg. 48,612, 48,617 (Dep't of Commerce Aug. 14, 2012), and noted that without the rule, the Board would be forced to "play archeologist with the record" for arguments that might have been made outside the parties' briefing, *id.* (citing *DeSilva v. DiLeonardi*, 181 F. 3d 865, 866–67 (7th Cir. 1999)).

3M Co. v. Evergreen Adhesives, Inc., 860 F. App'x 724, 725 (Fed. Cir. 2021).

Although the use of string citations in a petition may present various challenges, overall, we do not regard the Petition as exceeding reasonable limits of particularity and specificity. For example, as Patent Owner points out, in pages 38–39 of the Petition, in support of the argument that the JEDEC reference qualifies as prior art, Petitioner provides a long string citation to various deposition transcripts and declarations from prior *inter partes* review proceedings. *See* Prelim. Resp. 5. However, this particular string citation appears to generally be a summary of the testimonial evidence relied upon, which is broken out with more particularity and specificity in

the analysis that follows. Further, although Petitioner provides citations to the prior three *inter partes* proceedings involving the '623, '218, and '595 patents in the obviousness analyses, Petitioner has set forth, in this Petition, and outside of these citations, sufficient explanation and evidence relied upon to satisfy its burden at this stage of the proceeding. *See id.* at 5–6 (citing Pet. 40–41, 63, 67). As a practical matter, we do not find that cross-referencing to the Board's analysis in these prior proceedings violates the rules against incorporation by reference. However, Patent Owner's concerns are recognized, and Petitioner should be mindful going forward that we will not "play archeologist with the record."

IV. ANALYSIS OF CHALLENGES

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103 if "the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). An obviousness

determination based on a combination of references requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation.'"

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)); *see also Intelligent Bio-Sys.*, 821 F.3d at 1369. Therefore, to prevail in an *inter partes* review, Petitioner must explain how the proposed combination of prior art would have rendered the challenged claims unpatentable. At this preliminary stage, we determine whether the information presented in the Petition shows there is a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims would have been obvious over the proposed combination of prior art.

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art

> would have had a Bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer's memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system.

Pet. 11 (citing Ex. 1003 ¶ 55; Ex. 1102, 11–12; Ex. 1103, 11–12; Ex. 1034, 8–9). Patent Owner "applies Petitioner's proposed level of ordinary skill in the art." Prelim. Resp. 3–4. We find Petitioner's proposal is consistent with the level of ordinary skill in the art reflected by the prior art of record, and, therefore, adopt Petitioner's proposed level of ordinary skill in the art for purposes of this Decision. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

Petitioner contends that no claim construction is necessary. Pet. 23; Patent Owner does not address claim construction in the Preliminary Response. *See generally* Prelim. Resp. "The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the parties' arguments, we consider the scope of the claim requirements of first and second signaling interfaces, discussed in Section IV.D.4.n below.

D. Obviousness Over Hazelzet and JEDEC; Hazelzet and Buchmann; and Hazelzet and Wang

Petitioner contends that claims 1–20 are obvious over the combination of Hazelzet and JEDEC; Hazelzet and Buchmann; and Hazelzet and Wang. Pet. 39–109. For each combination, Petitioner asserts that the functionality of buffering data signals as taught in JEDEC, Wang, and Buchmann would be added to Hazelzet's memory module, that corresponding training would be added as taught in JEDEC, Wang, and Buchmann, and that the completion of the training sequences would be reported over Hazelzet's open-drain output. *Id.*

Aside from preliminarily addressing Patent Owner's arguments as to JEDEC's prior art status, we do not further address Petitioner's contentions for the combination of Hazelzet and JEDEC, or Petitioner's contentions for the combination of Hazelzet and Wang. Rather, we determine that Petitioner has sufficiently shown a reasonable likelihood it would prevail with respect to at least one challenged claim under the combination of Hazelzet and Buchmann.

1. Hazelzet (Ex. 1014)

Hazelzet was published on August 24, 2008 and is titled "High Density High Reliability Memory Module With Power Gating and a Fault Tolerant Address and Command Bus." Ex. 1014, codes (43), (54).

Hazelzet is generally directed to a high density, high reliability memory controller/interface. Ex. 1014 ¶ 7. Figure 2, reproduced below, is a block diagram of the enhanced server memory arrangement:

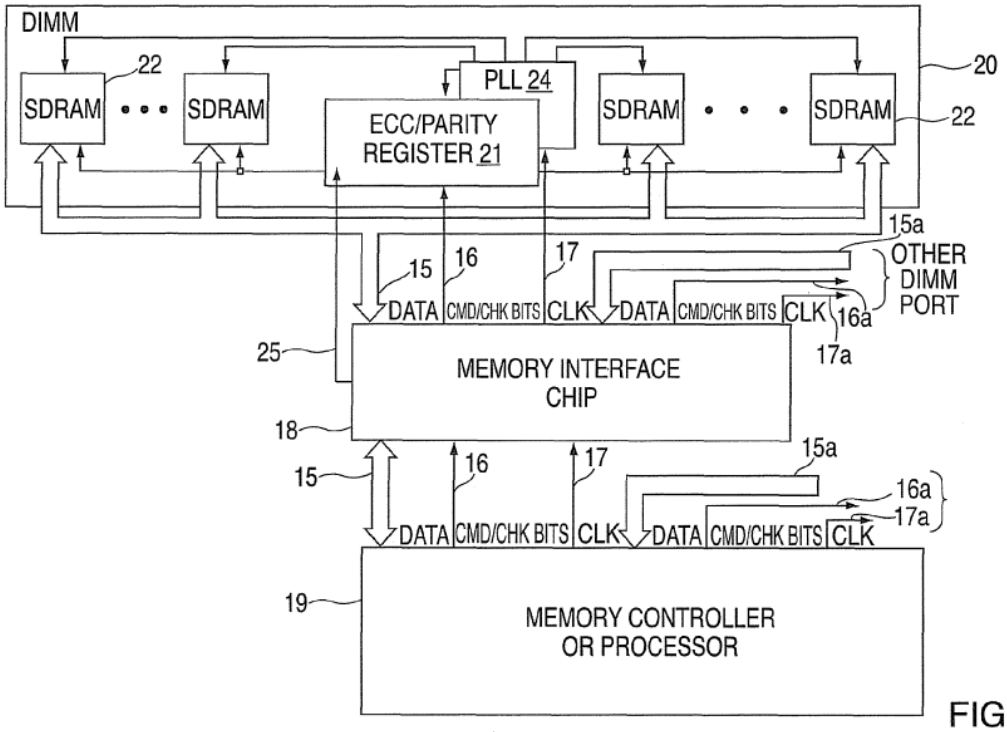

FIG. 2

Figure 2 depicts dual inline memory module ("DIMM") 20 with a "novel ECC/Parity Buffer chip 21" coupled to memory interface chip 18, which is coupled to memory controller or processor 19. *Id.* ¶ 38. Hazelzet describes that "DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins . . . are connected via the printed circuit to selected connectors 23 along the edge of both the back and front sides of the card." *Id.* ¶ 39. Figure 2 shows "the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16." *Id.* ¶ 38. "The memory interface chip 18 then sends and receives data, via line 15, to the memory devices, or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/Parity register chip 21 via line 25." *Id.*

Hazelzet further describes that the DIMM has "added error correction code logic (ECC) incorporated therein for correcting single bit errors while permitting continuous memory operation independent of the existence of these errors." Ex. 1014 ¶ 64. Hazelzet also discloses "[a] parity operating mode . . . to permit the system to interrogate the device to determine the error condition." *Id.* In this way, Hazelzet describes two modes: "ECC Mode (/ECC Mode low)" and "parity mode (/ECC Mode high)." *Id.* ¶¶ 69–70; *see also* Ex. 1014, Fig. 8. In addition, Hazelzet describes error reporting circuitry, where "[t]wo open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals)." *Id.* ¶ 72. "/Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error." *Id.*

2. JEDEC (Ex. 1015)

a. Description

The JEDEC reference is titled "Committee Letter Ballot" with subject "LRDIMM DDR3 Memory Initialization Chapter Proposal," and is a proposal to the JEDEC JC-40.4 committee for ballot approval. Ex. 1015 at 1; Ex. 1050 ¶ 7. The footer of the JEDEC reference states, "Ballot Template Version draft rev. F," and the word "Proposed" is vertically in red on the left margin. Ex. 1015.

JEDEC generally describes a "power-up initialization of the Memory Buffer." Ex. 1015 at 3. JEDEC discloses a training mode of MB-DRAM Training that includes two training sequences, "Write Leveling" and "Read

Enable Training." *Id.* at 8. JEDEC states that "[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODtn inputs must be kept low." *Id.* JEDEC describes that "training completion can be signaled by the assertion of ERROUT#." *Id.*

b. Whether the JEDEC Reference is Prior Art

Petitioner argues that the JEDEC reference was publicly accessible by November 11, 2009, and at least before June 13, 2010. Pet. 33–39. Patent Owner argues that Petitioner has not provided sufficient evidence to show that the JEDEC reference was publicly accessible before June 2009 or June 2010. Prelim. Resp. 32–54.

As will be discussed further herein, we determine that Petitioner has established a reasonable likelihood of prevailing on its challenge to at least one claim of the '319 patent for the Hazelzet and Buchmann, and Hazelzet, Buchmann, and Kim challenges. Therefore, we need not resolve this issue at this stage of the proceeding. Moreover, the parties' arguments as to whether the JEDEC reference is prior art raise numerous fact-intensive issues that are better resolved on a full record at trial. Therefore, in this section we will provide preliminary observations on the parties' positions.

Public accessibility is the "touchstone" in determining whether a document is a prior art printed publication. *SRI Int'l., Inc. v. Internet Sec. Systems, Inc.*, 511 F.3d 1186, 1194 (Fed. Cir. 2008) (emphasis omitted); *see also In re Lister*, 583 F.3d 1307, 1311 (Fed. Cir. 2009) (To qualify as a printed publication, a document "must have been sufficiently accessible to the public interested in the art."). "A reference will be considered publicly

accessible if it was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence[] can locate it." *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018) (internal quotation marks omitted); *Bruckelmyer v. Ground Heaters, Inc.*, 445 F.3d 1374, 1378 (Fed. Cir. 2006). In general, "[a]ccessibility goes to the issue of whether interested members of the relevant public could obtain the information if they wanted to." *Constant v. Advanced Micro–Devices, Inc.,* 848 F.2d 1560, 1569 (Fed.Cir.1988).

JEDEC is a standard-setting organization where, in the 2009-2010 timeframe, "virtually every company in the industry" was a member. Pet. 35, 36 (citing Ex. 1091,[3] 44:15–45:1, 45:19–47:19; Ex. 1050[4] ¶ 4; Ex. 1073[5]; Ex. 1074[6]). JEDEC technology proposals, such as the JEDEC reference, "originated in JEDEC task groups within committees." Ex. 2003[7] ¶ 10. The JEDEC reference is a committee ballot, where the proposal is elevated to the full committee for voting. *Id*. Committee members used an

[3] Deposition of John Halbert from IPR2022-00062, -00064 (July 22, 2022). Mr. Halbert, among other things, served as a representative for Intel Corporation at JEDEC from 2001–2003 and 2010–2017. Ex. 1054 ¶ 9.

[4] Declaration of Julia Carlson, who, among other things, works at JEDEC and has been involved with the standardization and publication activities of JEDEC since 1997. Ex. 1050 ¶¶ 2–3.

[5] JEDEC website page from The Wayback Machine, dated 4/10/2009, titled "Become a Member of JEDEC!"

[6] JEDEC website page from The Wayback Machine, dated 5/5/2009, titled "JEDEC Member Companies."

[7] Declaration of Dr. Feng Yang, who, among other things, held multiple senior leadership roles in JEDEC since 2005. Ex. 2003 ¶ 6.

internal JEDEC Voting Machine hosted on JEDEC's private intranet, which required a JEDEC login and password, to vote on ballots. *Id.* ¶¶ 11, 12. A ballot posted on JEDEC's Voting Machine could only be accessed by members of the JEDEC committee designated to vote on the ballot, or members of related JEDEC committees as needed. *Id.* ¶ 12. There is no dispute that the JEDEC reference was accessible to members of the JEDEC JC-40.4 committee. Pet. 37–38; Prelim. Resp. 34–35. The crux of the dispute is whether the JEDEC reference was publicly accessible to persons of ordinary skill in the art or other interested persons, aside from JEDEC members.

According to Petitioner, JEDEC permitted both company and individual members to join for a flat rate, and a person of ordinary skill in the art could "create a company" to join JEDEC. Prelim. Reply 5 (citing, e.g., Ex. 1048,[8] 1 & n.2; Ex. 1049,[9] 1 & n.2; Ex. 2004,[10] 23:23–25:10); Pet. 36–37. Petitioner contends that "[t]here is no evidence that JEDEC ever denied anyone membership." Pet. 37 (citing Ex. 1091, 43:9–20; Ex. 1073). Patent Owner, however, argues that JEDEC's membership is company based, limited to companies "that manufacture semiconductor products, or provide related services or equipment," and that pay a $4,000 a year fee. Prelim. Resp. 43 (citing Ex. 2003 ¶ 8; Ex. 1073; Ex. 1092,[11] 27:23–28:17).

[8] JEDEC Manual of Organization and Procedure, Revision of JM21N, May 2008 (May 2010).

[9] JEDEC Manual of Organization and Procedure, Revision of JM21N, December 2006 (May 2008).

[10] PTAB hearing transcript for IPR2022-00062 and -00064 (Feb. 15, 2023).

[11] Deposition of Julie Carlson from IPR2022-00062, -00064 (July 27, 2022).

Therefore, Patent Owner argues, an interested person "can't just join JEDEC." *Id.* (citing Ex. 2004, 23:23–24; Ex. 2003 ¶ 8).

There is conflicting evidence in the record as to whether individuals were permitted to join JEDEC. The JEDEC Manual of Organization and Procedure ("JEDEC Manual") states that "[a]ny company, organization, or *individual* conducting business that itself or through a related entity manufactures electronic equipment or electronic-related products, or provides electronics or electronics-related services, shall be eligible for membership in JEDEC." Ex. 1048, 1 (emphasis added); Ex. 1049, 1 (same). In contrast, the JEDEC website states that "Membership is company based, not by individual." Ex. 1073; *see also* Ex. 2003 ¶ 8 (testifying that "JEDEC membership is not (and never has been) available to individuals."); Ex. 1050 ¶ 5 (testifying that "[a]nyone interested can join JEDEC online, at JEDEC.org."). At this preliminary stage, we tend to agree with Petitioner that interested persons could join JEDEC, whether individually, or by creating a company. And likewise, that any interested member could join a committee. *See* Ex. 1048, 7 (stating that "Participation [in committees] shall be open to all persons who are directly and materially affected by the activity in question"); Ex. 1049, 6 (same); Ex. 1050 ¶ 5 (testifying that "[w]hen joining, any interested person can join any committee.").

There does not seem to be any dispute that JEDEC members have access to JEDEC documents. Thus, we focus our discussion on the public accessibility of the draft proposal in Exhibit 1015 to non-members. Petitioner contends that "JEDEC's meetings were publicized on the Internet and took place at hotels where anyone could walk in and observe the

presentations." Pet. 35 (citing Ex. 1071;[12] Ex. 1091, 33:5–37:17, 59:190–60:15). Petitioner also argues that JEDEC organized its committees and documents by technical area with a numbering convention, so a person of ordinary skill in the art "interested in that technical area could easily find the relevant JEDEC committee and its documents and meeting dates." *Id.* at 37. Petitioner further argues that "JEDEC also provided a search feature on its website to find documents," which could be searched by keyword, or "you could simply call the JEDEC office to help you find what you were looking for." *Id.* at 38 (citing, e.g., Ex. 1039; Ex. 1046,[13] 21–22; Ex. 1015; Ex. 1091, 53:3–54:18, 54:20–55:8; Ex. 1071).

Patent Owner argues that the JEDEC reference "was an internal, password-protected document only ever distributed and accessible to its authors." Prelim. Resp. 33. According to Patent Owner, the JEDEC reference is an internal "proposed" chapter authored by a JEDEC subcommittee that was never adopted by JEDEC; rather, a modified version was adopted as part of a standard that issued in 2014. *Id.* at 33–34 (citing Ex. 1015, 1–3; Ex. 1048, 7–8; Ex. 1049, 7; Ex. 2001;[14] Ex. 2002,[15] 15). Therefore, Patent Owner argues, the proposal is a draft that was not meant for public release, and was never published. *Id.* at 34, 37. Patent Owner further argues that such draft proposals are stored on internal JEDEC servers

[12] JEDEC website page from The Wayback Machine, dated 4/6/2009, titled "2009 Meetings Schedule."

[13] Meeting Minutes of JC-40 Digital Logic Committee, dated June 4, 2009.

[14] JEDEC Standard, LRDIMM DDR3 Memory Buffer (MB) Version 1.0, JESD82–30 (October 2014).

[15] Meeting Minutes of JC-40 Digital Logic Committee, dated December 10, 2009.

and are accessible only to relevant JEDEC committee members. Prelim. Resp. 35–36 (citing, e.g., Ex. 1051,[16] 1; Ex. 1050 ¶¶ 7–8; Ex. 1055[17] ¶¶ 6–7; Ex. 1048, 16–17; Ex. 1049, 16; Ex. 1037,[18] 21; Ex. 1092, 16:18–17:7, 18:23–21:17; Ex. 2003 ¶¶ 11–18). Further, Patent Owner argues, to access a ballot and proposal, JEDEC committee members must sign in with a login and password. *Id.* at 36 (citing Ex. 1092, 16:24–17:7, 19:3–9, 20:14–21:23; Ex. 2003 ¶¶ 11–18).

The current record supports that JEDEC's meetings were publicized on the Internet, but there is some dispute over whether they were open to the public. *See* Ex. 1071 (showing the JC-40 meeting on December 7–11, 2009 in Maui, HI); Ex. 2003 ¶ 9 (testifying that "[i]n 2009, JEDEC meetings were closed to the public"). However, the current record supports that non-members could attend meetings as a guest and also participate in committees. Ex. 1107, 178:23–179:18; Ex. 1048, 1 n. 2 (JEDEC Manual stating that "JEDEC membership is not a prerequisite to committee participation. Non-member participation fees will be charged."), 10 (stating that "All JEDEC committee and subcommittee meetings are open to members, their designated alternates, and guests invited by the committee or subcommittee chairperson"); Ex. 1049, 1 n. 2, 9 (same); Ex. 1046, 1–2 (meeting minutes of JC-40 Digital Logic Committee for June 4, 2009

[16] JEDEC Committee Letter Ballot proposal for LRDIMM DDR3 Memory Initialization, distributed November 11, 2009, expiring December 3, 2009.

[17] Declaration of Sung Joo Park, who, among other things, has represented Samsung at JEDEC for over fifteen years. Ex. 1055 ¶ 4.

[18] JEDEC Compilation of Tallies for JC-40 CMOS Digital Logic and point committees, generated on December 4, 2009.

showing "Members Present" and "Others Present"); Ex. 2002, 1–2 (meeting minutes of JC-40 Digital Logic Committee for December 10, 2009 showing "Members Present" and "Others Present"); *see Rambus Inc. v. Infineon Techs. Ag*, 318 F.3d 1081, 1085 (Fed. Cir. 2003) ("JEDEC meetings are open meetings, but nonmembers must receive an invitation to attend").

Given the foregoing, we do not find credible Mr. Yang's testimony that "JEDEC committee and subcommittee meetings are only open to members of the specific committee or subcommittee." Ex. 2003 ¶ 9. Rather, at this preliminary stage, the evidence tends to support that non-members could, at minimum, participate in committees and attend committee meetings. Although Patent Owner argues that Petitioner does not explain how an individual would have known to join the JC-40 committee (Prelim. Resp. 43), Petitioner submitted a page from the JEDEC website for the JEDEC Catalogue, showing JEDEC's naming conventions for documents and committees, including JC-40, which concerned CMOS Digital Logic. *See* Ex. 1072,[19] 59–61; Pet. 41. Moreover, the fact that meeting minutes in the record show "Others Present" supports that other people, outside of JEDEC members, were aware of the JC-40 Committee and its meetings. Ex. 1046, 1–2; Ex. 2002, 1–2.

Although non-members could participate in committees and attend committee meetings, it is not clear from the current record whether they would be provided JEDEC login and password information in order to access draft proposals stored on the internal JEDEC servers, or to access ballot proposals. *See* Ex. 1050 ¶ 5 (testifying that "joining members would

[19] JEDEC website page from The Wayback Machine, dated 4/21/2009, titled "JEDEC Catalogue."

have access to documents available to the committees and subcommittees the members join"); Ex. 1092, 16:24–17:7 (testifying that it is "correct" that "[o]nly JC-40 members would have access to that document on JEDEC's servers"); Ex. 2003 ¶ 11 (testifying that access to JEDEC's Voting Machine required a login and password), ¶ 12 (testifying that a ballot posted on JEDEC's Voting Machine can only be accessed using JEDEC-issued credentials by JEDEC committee members or members of related committees, but not members of the general public); ¶ 15 (testifying that login credentials are needed to access or view a ballot). However, minutes from JEDEC JC-40 committee meetings show that at committee meetings, ballots were reviewed, presentations[20] were shown, and task group updates were given, which indicates that non-members present at the committee meetings may have had access to proposals like the JEDEC reference, or at minimum, the proposals were discussed in the presence of non-members. Ex. 1046; Ex. 2002. Moreover, if a non-member could join a committee, it seems logical that the non-member would also have access to proposals and vote on the proposal. However, Patent Owner appears to be correct that there is no evidence in the record as to where the JEDEC reference could be found after the vote, and whether subsequently joined committee members, or anyone else, would have access to it. *See* Prelim. Resp. 44–45; *see Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1372 (Fed. Cir. 2019) (stating that "a work is not publicly accessible if the only people who know how to find it are the ones who created it").

[20] A presentation is an "initial showing or distribution of material proposed for publication." Ex. 1048, 14; Ex. 1049, 14. A June 2009 presentation for the Exhibit 1015 proposal is in the record as Exhibit 1039.

Further, the evidence in the record also supports that the JEDEC reference is a proposal that was never published by JEDEC. *See* Ex. 1048, 14 (describing the document development procedure, and stating that proposed material is approved for publication only after it "has successfully completed all of the above steps and obtained approval through the appropriate balloting process"); Ex. 1049, 14 (same); Ex. 2003 ¶ 9 (testifying that standards are only published after they have been approved by a full committee and ratified by the Board of Directors). As Patent Owner argues, the JEDEC reference was not adopted by JEDEC. Prelim. Resp. 33–34, 36–37 (citing Ex. 2001; Ex. 2002); Prelim. Sur-reply 5. Moreover, there is no evidence in the record that the JEDEC reference was ever published or made available on JEDEC's website. *See* Prelim. Resp. 50–51.

The parties also dispute whether proposals like the JEDEC reference were confidential. According to Petitioner, "[n]othing about JEDEC, its meetings, or its documents was confidential." Pet. 35 (citing Ex. 1054 ¶¶ 6, 11; Ex. 1091, 13:4–14:11, 32:11–20, 55:10–56:20). Patent Owner, on the other hand, argues that ballots "were treated as confidential within their respective committees, and it was 'contrary to JEDEC policy' to 'distribute a pending committee ballot to a non-JEDEC entity.'" Prelim. Resp. 36 (citing and quoting Ex. 1091, 23:3–18; Ex. 2003 ¶¶ 20–21). Patent Owner also argues that the JEDEC Manual "confirms that such documents are 'for internal use' only" and that "external use is permitted only 'at the discretion of the Board.'" *Id.* (citing Ex. 1049, 15; Ex. 1048, 15–16). Patent Owner also stresses that those having access to the proposal are creators or

collaborators, rather than consumers of the document. *See Id.* at 39, 46–47 n.13.

There are no confidentiality markings on the JEDEC reference, nor any statements in the JEDEC Manual regarding confidentiality restrictions. Although we recognize that "professional and behavioral norms" can give rise to an expectation that the information will not be copied or further distributed, *see Cordis Corp. v. Boston Sci. Corp.*, 561 F.3d 1319, 1333 (Fed. Cir. 2009), it is unclear whether this is the case here on the current record. We recognize that there is testimony that committee ballots[21] were treated as confidential (e.g., Ex. 2003 ¶¶ 20–21), but there is also testimony that proposals were freely discussed with third parties (e.g., Ex. 1091, 17–23). Patent Owner also requested a copy of the JEDEC reference, and submitted an email response from JEDEC that "JEDEC committee and task group materials and proposals, including but not limited to presentations, ballots, draft versions of standards, etc. are restricted to JEDEC members," (Prelim. Resp. 52; Ex. 2006), but even this email conflicts with JEDEC's own documents referred to above, which state that non-members may participate in committees and attend committee meetings. Further, the email response further asked "What is the purpose of your request?" so it is not clear that JEDEC would not provide the document if given further information. *See* Ex. 2006.

[21] The parties use the term "ballot" or "proposal" to refer to Exhibit 1015. Exhibit 1015 is titled "Committee Letter Ballot" and states that "[t]his ballot proposal is to specify LRDIMM DDR Memory Initialization and has been approved by DDR MBTG on 11/09/2009." Ex. 1015, 1.

Moreover, although the JEDEC Manual states that "guests and non-members must agree to comply with all JEDEC rules and procedures," (Ex. 1048, 1 n.2; Ex. 1049, 1 n.2), on this record, we are not apprised of any rules and procedures relating to confidentiality restrictions of proposals. We tend to agree with Petitioner that the "for internal use only" in the JEDEC Manual seems to refer to copyright restrictions, rather than confidentiality issues. *See* Pet. 36 n. 6; *see also* Ex. 1075[22] (stating that JEDEC members have "[p]ermission to reproduce JEDEC copyrighted works for internal company use without restriction"); *Weber, Inc. v. Provisur Techs., Inc.*, 92 F.4th 1059, 1062, 1068–69 (Fed. Cir. 2024).

Given the foregoing, factual issues remain as to how "accessible" the draft proposal in Exhibit 1015 would have been to an interested person who was not a member of JEDEC.

3. Buchmann (Ex. 1016)

Buchmann is titled "Power-On Initialization and Test for a Cascade Interconnect Memory System" and is generally directed to "[a] memory buffer, memory system and method for power-on initialization and test for a cascade interconnect memory system." Ex. 1016, codes (54), (57). Buchmann describes that "the memory buffer includes logic for executing a power-on and initialization training sequences initiated by the memory controller." *Id.* at code (57). Buchmann discloses that it "is operable in a static bit communication (SBC) mode and a high-speed mode." *Id.* at 1:43–55.

[22] JEDEC website page from The Wayback Machine, dated 4/13/2009, titled "Membership benefits."

Buchmann describes several training sequences, including training sequence TS0, which "is used to perform upstream (US) and downstream (DS) clock detection and repair (if necessary)." Ex. 1016, 5:51–53. During this training sequence, the memory module outputs various commands, including TS_done, which "indicates the local and all cascaded MBs are done with TS0." *Id.* at 6:1–20, Table 1. Buchmann also similarly describes other training sequences, TS2 and TS3. *Id.* at 7:15–8:45.

4. Independent Claim 1

Petitioner contends that the combination of Hazelzet and Buchmann teaches the limitations in independent claim 1. Pet. 50–81.

a. Motivation to Combine Hazelzet and Buchmann

Petitioner's proposed combination involves adding buffering data signal functionality to Hazelzet's memory module, and adding corresponding training, including training sequences like TS0 and TS3 in Buchmann, and reporting their completion with TS0_done or TS3_done as taught in Buchmann, over Hazelzet's open-drain output (UE 121). Pet. 40 (citing Ex. 1003 ¶¶ 191, 194–195; Ex. 1016, Figs. 4, 6, 5:51–7:2, Tables 1–2, 8:24–9:18, Tables 5–6). Petitioner argues that, in the combination, the module does not communicate any data or perform any normal read or write operations during the training operation. *Id.* at 41 (citing Ex. 1003 ¶¶ 68, 191). Petitioner submits that the Board has repeatedly relied on the Hazelzet/Buchmann combination to invalidate similar claims. *Id.* (citing Ex. 1034, 7–20; Ex. 1102, 15–44; Ex. 1103, 16–44).

Petitioner contends that Buchmann is analogous art to the '319 patent. Pet. 41–42. According to Petitioner, the combination is "merely an arrangement of old elements, such as data buffering, training, and reporting

techniques, with each performing its known function and yielding what one would expect without undue experimentation and with a reasonable expectation of success." *Id.* at 42 (citing Ex. 1003 ¶ 199).

Petitioner contends that a person of ordinary skill in the art would have been motivated to add data buffering and corresponding training to Hazelzet's memory module for various reasons, including (1) data buffering functionality was designed to be added to an RDIMM like Hazelzet's memory module for the well-known advantages of reduced load and increased performance and capacity; and (2) Hazelzet's emphasis on the need for initialization to achieve "improved overall system reliability." Pet. 42–44. Petitioner further contends that a person of ordinary skill in the art would have been motivated to combine Hazelzet and Buchmann by using training without normal memory read or write operations because training is designed to minimize errors for subsequent normal memory read and write operations. *Id.* at 45–47; *see id.* at 46 (stating that Buchmann's training would have complemented Hazelzet's initialization). Further, Petitioner contends that it would have been obvious to combine Hazelzet's open-drain output to report a status of Buchmann's training sequences for various reasons. *Id.* at 47–50.

b. Preamble [1(a)] "A memory subsystem operable with a system memory controller of a host system, comprising"

Petitioner contends that Hazelzet teaches the preamble.[23] Pet. 50–51. Specifically, Petitioner identifies Hazelzet's dual inline memory modules 20

[23] Petitioner does not argue that the preamble limits claim 1. Although we find that the evidence supports that the prior art teaches the preamble, we make no determination at this stage of the proceeding whether the preamble

("memory module) operable with Hazelzet's memory controller 19 ("memory controller of a host system"). *Id.* (citing Ex. 1003 ¶¶ 226–228; Ex. 1014, Figs. 2, 3A–3D, ¶¶ 36–39). Petitioner also identifies the equivalent limitations in the '623 patent (limitation [1.a], similar language), the '218 patent (limitation [1.a], same language), and the '595 patent (limitation [1.a], same language), and cites to the Board's analysis in the corresponding final written decisions. *Id.* at 56 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9; Ex. 1102, 44; Ex. 1103, 44).

c. Limitation [1(b)(1)] "dynamic random access memory elements on a printed circuit board and"

Petitioner contends that Hazelzet teaches limitation [1(b)(1)]. Pet. 51–53. Specifically, Petitioner identifies Hazelzet's SDRAMs on the printed circuit board (DIMM). *Id.* (citing Ex. 1003 ¶¶ 229–231; Ex. 1014 Figs. 2, 3A–3D, ¶¶ 15, 37, 39). Petitioner also identifies the equivalent limitations in the '623 claims [1.a], [1.d], and 2, '218 claims [1.b] and [1.c], and '595 claims [1.b] and [1.c]. *Id.* at 51 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex. 1102, 44–46; Ex. 1103, 44–45).

d. Limitation [1(b)(2)] "configurable to communicate data signals with the system memory controller; and"

Petitioner contends that the combination of Hazelzet and Buchmann teaches limitation [1(b)(2)]. Pet. 53–57. Specifically, Petitioner contends that, as shown in Figure 2, Hazelzet "discloses that its Memory Controller 19 communicates data with a memory interface chip 18 which "sends and

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of claim 1 is limiting. Similarly, we make no determination at this stage of the proceeding whether the preamble of claim 11 is limiting.

receives data from the DIMMs via the data line 15." *Id.* at 54 (citing Ex. 1003 ¶¶ 233; Ex. 1014, Fig. 2, ¶ 38).

Further, Petitioner contends that Buchmann discloses improvements to Hazelzet's data communication, including buffering the data signals. Pet. 54. Referring to annotated Figure 16 of Buchmann, Petitioner contends that Buchmann communicates data with the memory controller through a buffer using its Memory Device Data Interface according to address and control signals provided by its Memory Hub Control. *Id.* at 56–57 (citing Ex. 1016, Fig. 16, 21:20–60; Ex. 1003 ¶ 236).

Petitioner also identifies the equivalent limitations in the '623 claim [1.d], '218 claim [1.f], and '595 claim [1.f.ii]. Pet. 53 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–20; Ex. 1102, 47–50; Ex. 1103, 49).

e. Limitation [1(c)(1)] "a memory subsystem controller on the printed circuit board and"

Petitioner contends that Hazelzet teaches limitation [1(c)(1)]. Pet. 57–59. Specifically, Petitioner identifies Hazelzet's ECC/Parity register 21 on the printed circuit board (e.g., DIMM). *Id.* (citing Ex. 1003 ¶¶ 238–240; Ex. 1014, Figs. 2–3D, 4A–4B, 9, ¶¶ 32, 39, 41–42, 44). Petitioner also identifies the equivalent limitations in the '623 claims [1.a], [1.b], and [1.d], '218 claim [1.d], and '595 claim [1.d]. *Id.* at 57 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–20; Ex. 1102, 46–47; Ex. 1103, 45–46).

f. Limitation [1(c)(2)] "coupled to the dynamic random access memory elements,"

Petitioner contends that Hazelzet teaches limitation [1(c)(2)]. Pet. 60–61. Specifically, Petitioner contends that, as shown in Figure 2, Hazelzet's ECC/Parity Register 21 is coupled to SDRAMs 22. *Id.* (citing Ex. 1014, Figs. 2, 10, ¶¶ 15, 39, 42, 96; Ex. 1003 ¶¶ 241–243).

Petitioner also identifies the equivalent limitations in the '623 claim 2, '218 claim [1.d], and '595 claim [1.d]. Pet. 60 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex. 1102, 46–47; Ex. 1103, 45–46).

g. Limitation [1(c)(3)] "the memory subsystem controller having an open drain output,"

Petitioner contends that Hazelzet teaches limitation [1(c)(3)]. Pet. 61–63. Specifically, Petitioner contends that Hazelzet's ECC/Parity Register includes Error Logic 100 having an open drain output, including UE 121 to notify the system memory controller of uncorrectable or parity errors. *Id.* at 61 (citing Ex. 1014, Fig. 4B, ¶¶ 44, 59, 72; Ex. 1003 ¶¶ 244–247). Petitioner points to Hazelzet's disclosure that its open-drain outputs permit multiple modules to share a common signal line, with outputs driven low when the transistor gate receives a high voltage, and returns to a high impedance state when driven with a low/ground voltage. *Id.* at 63 (citing Ex. 1014 ¶¶ 72, 99; Ex. 1003 ¶¶ 246–247, 299).

Petitioner also identifies the equivalent limitations in the '623 claim [1.b], '218 claim [1.d], and '595 claim[1.d]. Pet. 61 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–20; Ex. 1102, 46–47; Ex. 1103, 45–46).

h. Limitation [1(d)(1)] "wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and"

Petitioner contends that Hazelzet teaches limitation [1(d)(1)]. Pet. 63–67. Specifically, Petitioner relies on the above-described ECC/Parity Register including Error Logic 100 having an open drain output, including UE 121 to notify the system memory controller of parity errors via parity error signals PERR 111. *Id.* at 63–64 (citing Ex. 1014, Fig. 4B, ¶¶ 59, 70, 72, 76; Ex. 1003 ¶¶ 248–254). Petitioner points out that when the

memory module is in the "parity mode," parity generator/checker circuit 231 generates and sends the parity error signal (PERR) to Error Logic 100. *Id.* at 64 (citing Ex. 1014, Figs. 4B, 5, ¶¶ 59, 70, 72, 76). The parity error is reported via the Uncorrectable Error (UE) line in response to the ECC/Parity register receiving address and command signals and corresponding check bits. *Id.* at 65–66 (citing Ex. 1014, Figs. 2, 8, ¶¶ 18, 38, 72, 99; Ex. 1003 ¶¶ 249–251). Petitioner argues that one of ordinary skill would have understood that parity reporting was based on normal memory read and write operations. *Id.* at 66–67 (citing Ex. 1014, ¶ 109; Ex. 1056, 33; Ex. 1003 ¶¶ 252–254).

Petitioner also identifies the equivalent limitations in the '623 claims [1.b], 2, 7, and 9, '218 claims [1.f], [1.h], and 5, and '595 claims [1.e.ii], [1.f.iii], and 5. Pet. 63 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex. 1102, 47–52, 64–66; Ex. 1103, 46–47, 50, 69–71).

i. Limitation [1(d)(2)] "a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations;"

Petitioner contends that the combination of Hazelzet and Buchmann teaches limitation [1(d)(2)]. Pet. 67–74. Specifically, Petitioner contends that the combination teaches providing a status signal to the memory controller via Hazelzet's open drain output during an initialization operation about the status of training sequences, which would have been understood to occur before, and thus to be distinct from, the parity error reporting interface. *Id.* at 67–68 (citing Ex. 1014, Fig. 4B, 5, ¶¶ 59, 70, 72, 76; Ex. 1003 ¶¶ 256–257). Petitioner relies on Buchmann's Memory Buffer that performs and reports completion of "TS0 and TS3 training in an SBC (error correcting) mode during initialization before the high-speed normal operations." *Id.* at 69 (citing Ex. 1016, Figs. 4, 6, 3:52–54, 5:6–22, 4:51–12:59, 5:51–7:2 & Tables 1–2, 8:24–9:18 & Tables 5–6, 14:1–15:15). Petitioner argues that one of ordinary skill would have understood that the "second" interface for indicating the completion of Buchmann's training during initialization was distinct from Hazelzet's first interface indicating parity errors in commands received from the host during subsequent normal operations. *Id.* (citing Ex. 1003 ¶ 261).

Petitioner further argues that the combination of Hazelzet and Buchmann renders obvious that the initialization operation is distinct from any of the normal operations, given that Buchmann teaches performing its TS0 and TS3 training during power-on initialization without any normal operations, such as normal memory read and write operations. *Id.* at 69–70

(citing Ex. 1016, Abstr., 5:51–6:50 (including Table 2), 8:24–9:18 (including Table 6); Ex. 1003 ¶ 264). Petitioner also argues that a person of ordinary skill in the art would have been motivated to use Hazelzet's open-drain output to indicate completion of the training to the controller so that it can perform normal memory read and write operations reliably. *Id.* at 73–74 (Ex. 1003 ¶¶ 268–269).

Petitioner also identifies the equivalent limitations in the '623 claims [1.c], 2, and 8, '218 claims [1.e.ii], [1.f], [1.i], 4, and 7, and '595 claims [1.e.iii], [1.g], [10.g], and 7. Pet. 67 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex. 1102, 47–50, 52–53, 63–64, 67–68; Ex. 1103, 47–48, 50–52, 56, 73–74).

> *j. Limitation [1(e)(1)] "wherein, during the normal memory read or write operations, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and"*

Petitioner contends that Hazelzet teaches limitation [1(e)(1)]. Pet. 74–77. Specifically, Petitioner contends that Hazelzet's memory controller 19 sends address and command information through memory interface chip 18 to register chip 21 via add/cmd line 16, and the register chip drives the address and command signals via buffer circuits to the memory devices during normal memory read or write operations. *Id.* at 75–77 (citing Ex. 1014, Figs. 2, 4A–B, ¶¶ 15, 24, 35, 38, 41, 44, 68, 73, 84; Ex. 1003 ¶¶ 270–276). Petitioner further contends that Hazelzet's SDRAM memories communicate data signals with the memory controller in accordance with the address and command signals of the corresponding read

or write operations. *Id.* at 77 (citing Ex. 1014, Fig. 2, ¶¶ 15, 35, 38, 41, 64, 70; Ex. 1003 ¶¶ 274–276).

Petitioner also identifies the equivalent limitations in the '623 claims [1.d] and 2, '218 claims [1.f], [1.g.i], and [1.g.ii], and '595 claims [1.f.i] and [1.f.ii]. Pet. 74–75 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex. 1102, 47–51; Ex. 1103, 48–49).

> *k. Limitation [1(e)(2)] "the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the normal memory read or write operations; and"*

Petitioner contends that Hazelzet teaches limitation [1(e)(2)]. Pet. 78–79. Petitioner contends that, when in parity mode, Hazelzet's ECC/Parity Register has open-drain output UE 121 to indicate a parity error using parity generator/checker circuit 231 and error logic circuit 100. *Id.* (citing Ex. 1014, Fig. 8, ¶¶ 18, 59, 64, 70, 72, 76, 99; Ex. 1003 ¶¶ 277–280).

Petitioner also identifies the equivalent limitations in the '623 claims [1.b], 2, 7, and 9, '218 claims [1.f], [1.h], and 5, and '595 claims [1.e.ii], [1.f.iii], and 5. Pet. 78 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex. 1102, 47–52, 64–66; Ex. 1103, 46–47, 50, 69–71).

> *l. Limitation [1(e)(3)] "wherein, during the initialization operation, the memory subsystem controller is configured to output via the open drain output a signal related to one or more parts of the initialization operation sequences."*

Petitioner contends that the combination of Hazelzet and Buchmann teaches limitation [1(e)(3)]. Pet. 80–81. Petitioner contends that, in the proposed combination, Hazelzet's ECC/Parity register, modified in view of Buchmann, is configured to output, via the open drain output, signals related to the status of respective training sequences as part of the initialization

operation, such as signals indicating the status of Buchmann's TS0 or TS3 training. *Id.* at 80 (citing Ex. 1003 ¶¶ 281–286). In the combination, the open-drain output would be at a low logic level to indicate the respective training sequences were in progress, and the open-drain output would be in a high impedance state so that the logic level of the open-drain output can be pulled high by a pull-up resistor when those operations completed in each memory module. *Id.*

Petitioner also identifies the equivalent limitations in the '623 claims [1.c] and 8, '218 claims [1.e.ii], [1.i], and 4, and '595 claims [1.g], 7, and [10.g]. Pet. 80 (citing Ex. 1003 ¶¶ 156–158; Ex. 1034, 9–21; Ex. 1102, 47, 52–53, 63–64; Ex. 1103, 50–52, 73–74).

m. Patent Owner's Arguments

Patent Owner argues that Petitioner fails to demonstrate that the asserted combinations teach the independent claim 1 and 11 requirements of a "second signaling interface" that is "distinct from" a "first signaling interface." Prelim. Resp. 22–30. Patent Owner argues that neither Petitioner nor its expert identify the "interface circuitry" that satisfies these claim requirements. *Id.* Patent Owner asserts that "Petitioner maps unspecified 'interface circuitry' in Hazelzet's ECC/Parity register 21 to the claimed 'first signaling interface,'" and fails to "identify[] a second, distinct signaling interface." *Id.* at 25, 27. Patent Owner further argues that, in setting out its rationale for the combination of Hazelzet and Buchmann, Petitioner does not allege that it would have been obvious to modify Hazelzet to include two distinct signaling interfaces. *Id.* at 26 n. 8. Patent Owner therefore argues:

> Petitioner thus posits what the two alleged signaling interfaces in its proposed combinations would communicate

> (parity errors for the first interface training status for the second interface), but fails to demonstrate that Hazelzet's "interface circuitry" or any other combination of the alleged prior art actually includes the two, distinct signaling interfaces that are recited in the claims.

Prelim. Resp. 27–28. Patent Owner also argues that Petitioner has failed to "explain what a POSITA would have understood the term 'interface' or 'signaling interface' to mean." *Id.* at 28. At most, argues Patent Owner, Petitioner attempts to map the same (unspecified) interface circuitry onto both the first and second interface claim requirements, despite the requirement that they be two distinct interfaces. *Id.*

As a separate challenge to Petitioner's reliance on the combination of Hazelzet and Buchmann, Patent Owner argues that Petitioner improperly relies on collateral estopped for its challenges instead of making the necessary evidentiary showings in the Petition, despite the fact (according to Patent Owner) that collateral estoppel does not apply to this case. Prelim. Resp. 54–55.

n. Analysis

We disagree that Petitioner has not demonstrated that the combination of Hazelzet and Buchmann teaches the independent claim 1 and 11 requirements of a "second signaling interface" that is "distinct from" a "first signaling interface." For the first interface, Petitioner identifies Hazelzet's disclosure of parity error signal PERR 111 applied, during parity mode, to open drain output UE 121, indicating a parity error. Pet. 63–67; Ex. 1014, Fig. 4B, ¶¶ 59, 70, 72, 109. For the second interface, Petitioner identifies, in the Hazelzet/Buchmann combination, a separate status signal applied, during initialization, to open drain output UE 121 reporting completion of TS0 and

TS3 training in an SBC (error correcting) mode during initialization of a memory buffer incorporated into the Hazelzet memory module. Pet. 40, 67–68, 69.

Although Patent Owner argues that Petitioner has failed to identify detailed "interface circuitry," the claims are only directed to ***providing*** distinct first and second signaling interfaces ***via the open drain output***. This not a reference to interface circuitry — it makes no sense to "provide" circuitry "via the open drain output." Rather, two distinct interface ***signals*** are provided via the open drain output. The '319 patent, referring to the second interface, states that "a handshake mechanism based on notification ***signaling*** . . . can be implemented by adding a new interface (notifying) **signal** between the [system memory controller] and the memory subsystem controller [which] can be an open drain signaling from the memory subsystem controller to the [system memory controller]." Ex. 1001, 4:6-16 (emphasis added). The patent describes the first interface as a "parity error" signal applied to an "error-out pin" during "operation mode," where the error-out pin is coupled to the same open drain signaling. *Id.* at 8:26–31, 11:19–21. These two distinct interface signals are shown in Figure 3, discussed above at page 8, as task in progress signal 44 in initialization mode and parity error signal 46 in operational mode. *Id.* at Fig. 3, 11:15–29. This directly corresponds to the TS0 and TS3 training signals and parity error signal PERR 111 of the Hazelzet/Buchmann combination on which Petitioner relies.

We also disagree with Patent Owner's argument that Petitioner's reliance on collateral estoppel is unjustified. Although Petitioner provides citations to what Petitioner contends are the relevant portions in the final

written decisions in IPR2018-00303, IPR2022-00062, and IPR2022-00064, Petitioner also provides explanation and citations to relevant evidence for its contentions in the Petition, as described above. *See* Pet. 39–81. Petitioner provides a claim analysis of the combined teachings of the references against the subject matter of claim 1, and provides citations to what Petitioner contends are the relevant portions in the final written decisions in IPR2018-00303, IPR2022-00062, and IPR2022-00064. *Id.*

In sum, we have reviewed Petitioner's contentions, including the relevant portions of the prior *inter partes* review proceedings, and Patent Owner's arguments. For the reasons set forth by Petitioner, on the current record, we determine that the information presented in the Petition demonstrates a reasonable likelihood that claim 1 is unpatentable over Hazelzet and Buchmann.

5. Claims 2–20

Petitioner argues claims 2–20 are unpatentable over the combination of Hazelzet and JEDEC; Hazelzet and Buchmann; and Hazelzet and Wang. combination of Hazelzet and Buchmann. Pet. 81–109. Claim 11 is an independent method claim with similar limitations to claim 1. *See* Ex. 1001, 15:61–16:23. Claims 2–10 depend from claim 1, and claims 12–20 depend from claim 11. *Id.* at 15:5–60, 16:24–17:12.

As discussed above, Petitioner has demonstrated a reasonable likelihood of success in proving that at least claim 1 of the '319 patent is unpatentable over Hazelzet and Buchmann, and we institute on all challenges raised in the Petition. *See SAS Inst., Inc. v. Iancu*, 584 U.S. 357, 362 (2018); *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute to require "a simple yes-or-

no institution choice respecting a petition, embracing all challenges included in the petition"); 37 C.F.R. § 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.").

We have, however, reviewed Petitioner's contentions with respect to the unpatentability of claims 2–20 over Hazelzet and Buchmann. *See* Pet. 81–109. Petitioner provides a claim analysis of the combined teachings of the references against the subject matter of claims 2–20, and also provides citations to what Petitioner contends are the relevant portions in the final written decisions in IPR2018-00303, IPR2022-00062, and IPR2022-00064. *Id.*

At this stage of the proceeding, unless as otherwise set forth in this Decision, Patent Owner does not dispute Petitioner's contentions as to the obviousness of claims 2–20 over the combination of Hazelzet and Buchmann. *See generally* Prelim. Resp.

We determine, on the current record, for the reasons set forth by Petitioner, that the information presented in the Petition demonstrates a reasonable likelihood that claims 2–20 are unpatentable over Hazelzet and Buchmann.

E. Obviousness Over Hazelzet, JEDEC, and Kim; Hazelzet, Buchmann, and Kim; and Hazelzet, Wang, and Kim

Petitioner alternatively contends that claims 1–20 would have been obvious over the combination of Hazelzet, JEDEC, and Kim; Hazelzet, Buchmann, and Kim; and Hazelzet, Wang, and Kim. Pet. 110–115. For each combination, Petitioner asserts that Kim's open-drain transistor

functionality would be included within Hazelzet's error logic 100. *Id.* at 112. We do not further address Petitioner's contentions for the combination of Hazelzet, JEDEC, and Kim, or Petitioner's contentions for the combination of Hazelzet, Wang, and Kim. Rather, we determine that Petitioner has sufficiently shown a reasonable likelihood it would prevail with respect to at least one challenged claim under the combination of Hazelzet, Buchmann, and Kim.

1. Kim (Ex. 1017)

Kim is titled "Providing a Memory Device Having a Shared Error Feedback Pin" and is generally directed "to a memory device having a shared error feedback pin." Ex. 1017, code (54), 1:6–8. Kim's Figure 4 is reproduced below.

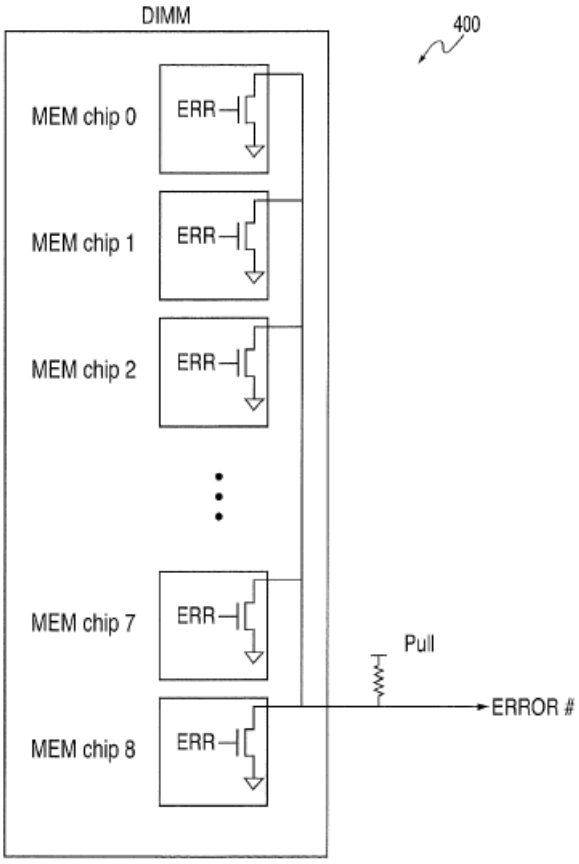

FIG. 4

Kim's Figure 4 shows "a block diagram of a memory module [400] having an error feedback pin that is shared among multiple device[s]." Ex. 1017, 3:13–16. Kim's Figure 4 further depicts "the error output line from the memory devices are dotted together via open drain drivers to a single error line that is output from the memory module 400." *Id.* at 6:1–3.

Kim's Figure 5 is reproduced below.

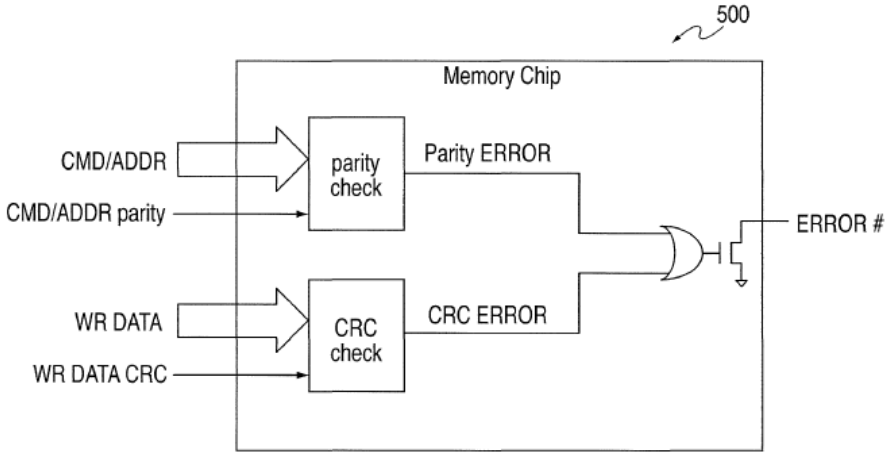

FIG. 5

Kim's Figure 5 depicts "a block diagram of a memory device 500 that shares an error feedback pin between data CRC and address parity." Ex. 1017, 6:13–15.

2. Analysis

Petitioner's contentions for claims 1–20 are the same as in the Hazelzet/Buchmann ground, except that Petitioner further asserts that Kim's open-drain transistor functionality would be included within Hazelzet's error logic 100. Pet. 112. In addition, Petitioner cites to the portions of the Board's analysis in IPR2018-00303, IPR2022-00062, and IPR2022-00064 that it contends are applicable. *Id.* at 110 (citing Ex. 1034, 20–21; Ex. 1102, 71–75; Ex. 1103, 78–82).

Petitioner relies on Kim's "open drain output (ERROR#) with an output pin coupled to the drain of a transistor having a gate, source, and a drain," as shown in Figure 4 of Kim. Pet. 110; *see* Ex. 1003 ¶ 292. Petitioner further asserts that Kim "discloses using a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor." Pet. 111 (citing Ex. 1017, Fig. 5, 6:13–18; Ex. 1003 ¶ 293).

Petitioner asserts that:

> In the combination, Kim's open-drain transistor functionality would be included within Hazelzet's error logic 100 such that signals indicating parity mode error, ECC mode error, and training status would be provided to a logic gate, e.g., Kim's OR gate, which would select among them based on the module's mode, as in Hazelzet. The output of the OR gate would be coupled to drive an open-drain transistor's gate, which itself drives UE 121. . . .

Id. at 112.; *see also id.* at 113 (depicting annotated figure showing the combination); Ex. 1003 ¶ 294. Petitioner explains that the combination would result in the transistor configurations, signaling, and logic elements as recited in the claims. Pet. 113–114 (citing Ex. 1003 ¶¶ 214–223, 294, 296–300; Ex. 1017, Fig. 4, ¶ 99).

Petitioner contends that Kim is analogous art to the '319 patent, and provides various reasons for the combination with Hazelzet. Pet. 114–115. For example, Petitioner argues that using Kim's output-pin functionality in Hazelzet's system "would have achieved predictable results, i.e., using an open drain-output to provide error or status information from multiple components." *Id.* at 114 (citing Ex. 1003 ¶ 301). Petitioner also argues that a person of ordinary skill in the art would have bene motivated to use Kim's open-drain techniques "because it represented a well-known, reliable, and simple technique to provide error and/or status information from a number of components." *Id.* at 114–115 (citing Ex. 1014 ¶¶ 72, 122; Ex. 1017, Figs. 4–5, 5:65–6:18, 12:18–23; Ex. 1003 ¶ 303). Moreover, Petitioner argues that it would have been obvious to implement Kim's open-drain output in this fashion, and also for a person of ordinary skill in the art to use

an OR gate as in Kim, or a multiplexor, within Hazelzet's Error Logic 100 to select which signal to drive the open-drain output. *Id.* at 115.

Patent Owner repeats its arguments, discussed above, that Petitioner does not demonstrate that the asserted combinations teach the independent claim 1 and 11 requirements of a "second signaling interface" that is "distinct from" a "first signaling interface." Prelim. Resp. 30–31. Patent Owner submits that Petitioner does not point to anything in Kim that would further support its arguments regarding these claim requirements. *Id.* To the contrary — as discussed above, Kim provides an example in the form of an OR-gate that alternatively applies a "Parity ERROR" or "CRC ERROR" signal to an open drain output "Error #" to provide error information, and Petitioner demonstrates that the Hazelzet/Buchmann/Kim combination would extend this arrangement to also include a distinct training status signal. Pet. 112-113. This provides further support of Petitioner's challenges to the claims.

In sum, we have reviewed Petitioner's contentions, including the relevant portions of the prior *inter partes* review proceedings, and Patent Owner's arguments. For the reasons set forth by Petitioner, on the current record, we determine that the information presented in the Petition demonstrates a reasonable likelihood that claims 1–20 are unpatentable over Hazelzet, Buchmann, and Kim.

V. CONCLUSION

For the above reasons, we determine that the information presented in the Petition shows a reasonable likelihood that claims 1–20 of the '319 patent are unpatentable as obvious over Hazelzet and Buchmann and Hazelzet, Buchmann, and Kim. Because Petitioner demonstrates that at least

one claim of the '319 patent meets the threshold for institution, we, therefore, institute *inter partes* review on all claims and grounds as challenged in the Petition. 37 C.F.R. § 42.108(a) ("When instituting . . . review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."); *SAS*, 138 S. Ct. at 1359–60.

VI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that *inter partes* review of claims 1–20 of U.S. Patent No. 11,880,319 B2 is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of U.S. Patent No. 11,880,319 is instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is given of the institution of a trial.

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