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Paper 9
Date: November 8, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.,
Petitioner,

v.

THE TRUSTEES OF PURDUE UNIVERSITY,
Patent Owner.

IPR2022-00723
Patent 7,498,633 B2

Before GRACE KARAFFA OBERMANN, JO-ANNE M. KOKOSKI, and JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Petitioner filed a Petition (Paper 3, "Pet.") for institution of an *inter partes* review of claims 1–8 and 12–15 of U.S. Patent No. 7,498,633 B2 (Ex. 1001, "the '633 patent"). Patent Owner filed a Preliminary Response. Paper 8 ("Prelim. Resp."). This Decision is based solely on the information presented in the Petition and Preliminary Response.

A. Real Parties-in-Interest

The Petition identifies STMicroelectronics, Inc., STMicroelectronics N.V., and STMicroelectronics International N.V. as real parties-in-interest for Petitioner. Pet. 1. Patent Owner's Mandatory Notice identifies "The Trustees of Purdue University and the Purdue Research Foundation" as real parties-in-interest for Patent Owner. Paper 5, 1.

B. Related Matters

Both parties identify as related matters the co-pending district court litigation in *The Trustees of Purdue University v. STMicroelectronics N.V. et al.*, No. 6:21-CV-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.). Pet. 1–2; Paper 5, 1. Patent Owner, but not Petitioner, also identifies IPR2022-00761 ("IPR761") as a related matter. Paper 4, 1; *cf*. Pet. 1–2. Concurrently herewith, we issue a decision denying institution of review in IPR761.

In addition, we take note that Petitioner previously filed a petition for review of claims 9–11 in IPR2022-00252 ("IPR252"), based on the same prior art references asserted in the instant Petition. The Board denied that request in a decision entered on June 22, 2022. IPR252, Paper 13.

II. BACKGROUND

A. The '633 Patent (Ex. 1001)

The '633 patent relates to a double-implanted metal-oxide semiconductor field effect transistor ("DIMOSFET") having, among other features, a silicon-carbide substrate, a drift semiconductor layer, a current spreading semiconductor layer formed on a front side of the drift semiconductor layer, and a junction field-effect transistor ("JFET") region formed on a front side of the current spreading semiconductor layer. Ex. 1001, 8:56–9:14, 10:19–10:40. In some embodiments, the substrate has "a first concentration of first type impurities" and the "drift semiconductor layer" has "a second concentration of first type impurities less than the first concentration." *Id*. at 8:58–63.

"[T]he current spreading semiconductor layer may be a concentration of first type impurities that is at least one order of magnitude greater than the concentration of first type impurities of the drift semiconductor layer." *Id*. at 3:2–6. We reproduce below Figure 1 from the '633 patent.

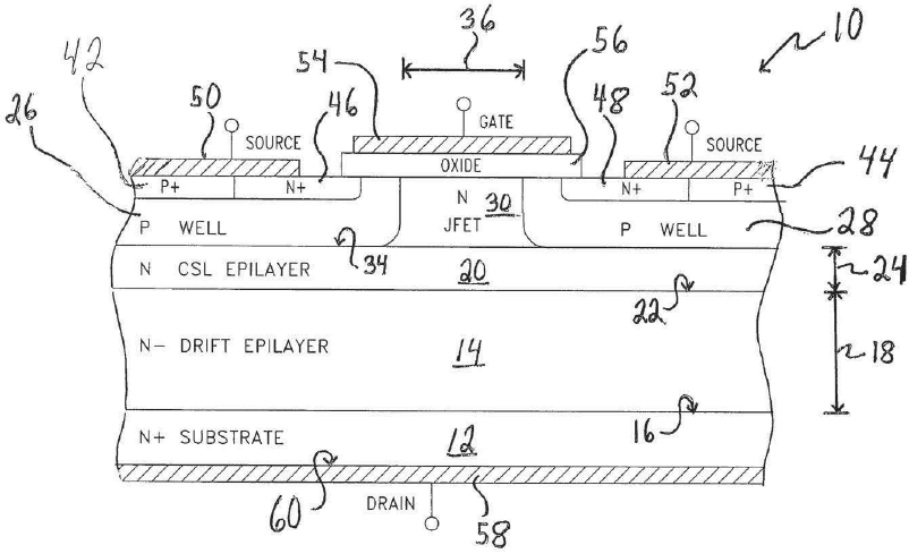


Fig. 1

Ex. 1001, Fig. 1. Figure 1 is a diagrammatic cross-sectional view of an embodiment of semiconductor device 10. *Id*. at 3:50–51.

To be clear, Figure 1 illustrates current spreading semiconductor layer 20 ***formed on*** a front side of drift semiconductor layer 14, where JFET region 30 is ***formed on*** a front side of current spreading layer 20. *Id*. at 5:1–26. Independent claims 1 and 12 both specify that relationship between those structural features. *Id*. at 8:56–9:14, 10:19–40. This Decision turns on the sufficiency of Petitioner's information as to whether the prior art would have suggested a MOSFET having "a current spreading semiconductor layer" as claimed in the '633 patent. Ex. 1001, 8:64. Our analysis focuses on the current spreading layer limitation, including the specified relationship of that layer to the JFET region and drift semiconductor layer.

B. Challenged Claims

We reproduce below independent claim 1.

> 1. A metal-oxide semiconductor field-effect transistor comprising:
>
> a silicon-carbide substrate having a first concentration of first type impurities;
>
> a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;
>
> ***a current spreading semiconductor layer formed on a front side of the drift semiconductor layer***;
>
> a first source region;
>
> a second source region;
>
> ***a JFET region formed on a front side of the current spreading semiconductor layer*** and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities;

> a plurality of source regions; and
> a plurality of base contact regions,
> wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

Ex. 1001, 8:56–9:14 (Board's emphasis). Similarly, independent claim 12 requires, among other things, "a current spreading semiconductor layer formed on a front side of the drift semiconductor layer" and a "JFET region ***being formed*** on a front side of the current spreading semiconductor layer." *Id*. at 10:25–26, 10:31–32 (Board's emphasis, highlighting a slight difference between the terms in claim 1 and claim 12).

Each of the dependent claims inherits the current spreading semiconductor layer limitation of claim 1 or claim 12. Thus, we focus our analysis on the dispositive question of whether Petitioner shows sufficiently, for purposes of trial institution, that the asserted prior art would have suggested a MOSFET that includes a current spreading semiconductor layer as specified in the independent challenged claims.

C. Asserted Ground of Unpatentability

Petitioner advances a single ground of unpatentability based on information that the subject matter of claims 1–8 and 12–15 would have been obvious under 35 U.S.C. § 103(a)[1] over the combined disclosures of

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the '633 patent has an effective filing date before March 16, 2013 (Ex. 1001, codes (22), (60), (65)), we refer to the pre-AIA version of Section 103.

Ryu[2] (Ex. 1003) and Williams[3] (Ex. 1004). Pet. 4. The challenge is supported by the Declaration of Dr. Vivek Subramanian (Ex. 1035).

III. ANALYSIS

We have authority to institute an *inter partes* review only where "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). The findings and conclusions set forth in this Decision are provided solely for the purpose of explaining our determination that Petitioner has not met that standard on this record.

A. Overview of the Prior Art

1. Ryu (Ex. 1003)

Ryu is titled "Vertical JFET Limited Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors and Methods of Fabricating Vertical JFET Limited Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors." Ex. 1003, code (54). Ryu is concerned with "semiconductor devices" such as silicon carbide (SiC) MOSFETs. *Id.* ¶ 3.

Ryu discloses an embodiment in which "a lightly doped n^- drift layer 12 of silicon carbide is on an optional n^+ layer 10 of silicon carbide." *Id*. ¶ 40. We reproduce below Ryu's Figure 2A.

[2] U.S. Patent Application Publication No. 2004/0119076 A1, published June 24, 2004, filed October 30, 2003.

[3] U.S. Patent 6,413,822 B2, issued July 2, 2002, filed April 22, 1999.

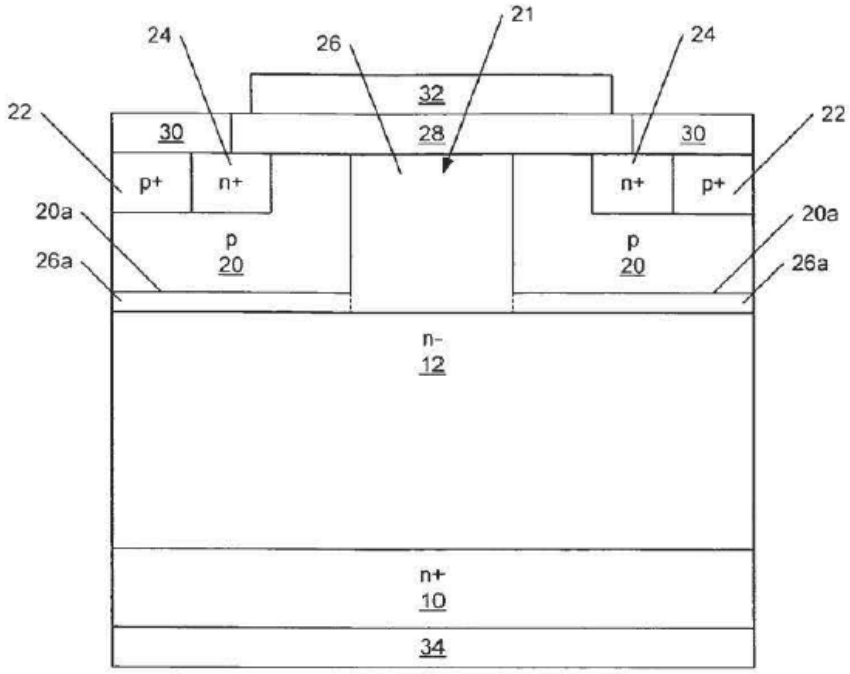


Figure 2A

Ex. 1003, Fig. 2A. Figure 2A of Ryu "is a cross-sectional view of a SiC MOSFET" and illustrates substrate layer 10 made of SiC and doped to an "n^+" concentration. *Id.* ¶¶ 28, 40. Drift layer 12 on substrate layer 10 may be an epitaxial layer of SiC and doped to an "n^-" concentration. *Id.* The gap between p-wells 20 "may be referred to as the JFET region 21." *Id.* ¶ 44. Ryu discloses that "p-wells 20 are implanted so as to extend into but not through the region 26." *Id.* ¶ 42.

Of critical significance to our analysis, Petitioner directs us to no disclosure in Ryu, and we discern none, that discloses a current spreading layer. *See generally* Pet.; Ex. 1003 (Ryu, especially Figure 2A).

2. Williams (Ex. 1004)

Williams is titled "Super-Self-Aligned Fabrication Process of Trench-Gate DMOS With Overlying Device Layer." Ex. 1004, code (54). The disclosure of Williams is not discussed in our analysis of the challenges.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)). In determining the level of skill in the art, we consider evidence of the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus. Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner directs us to Dr. Subramanian's opinion that a person of ordinary skill in the relevant technical field at the time of the invention "would have had the equivalent of a Bachelor's [D]egree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices." Pet. 3; Ex. 1035 ¶ 23. In Petitioner's and Dr. Subramanian's further view, "Less work experience may be compensated by a higher level of education, such as a Master's Degree, and vice versa." Pet. 3; Ex. 1035 ¶ 23.

Patent Owner counters, "Petitioner's asserted level of skill in the art is absurdly low given the silicon carbide technology" that is the subject of the '633 patent. Prelim. Resp. 17. In Patent Owner's view, the ordinarily skilled artisan would have possessed a Master's Degree in electrical engineering or a related field "with a concentration in design and fabrication of silicon carbide power semiconductor devices" or a Bachelor's Degree in

electrical engineering or a related field combined with "two years of experience in design and fabrication of silicon carbide power semiconductor devices." *Id*. at 18–19. Patent Owner directs us to evidence that "[t]his level of ordinary skill is consistent with the specialized nature of the field of silicon carbide power semiconductor devices." *Id*. at 19; Ex. 2004, x. Patent Owner further advances evidence that the '633 patent inventors, as well as a "few others who were active in the highly specialized field of silicon carbide power devices," possessed backgrounds consistent with Patent Owner's proposed narrower definition of the level of ordinary skill. Prelim. Resp. 20; Ex. 2007, 1–2, 19; Ex. 2017, 1; Ex. 2018, 1; Ex. 2019, 1–2.

On this record, we determine that the level of ordinary skill is reflected in the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) ("the prior art itself" may "reflect[] an appropriate level and a need for testimony is not shown" (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp*., 755 F.2d 158, 163 (Fed. Cir. 1985))). A more specific definition is not necessary, for purposes of deciding whether to institute review, at least because neither party explains how the result would change based on our selection of a definition. To the extent a more specific definition is required, however, we adopt Petitioner's proposed definition, which is consistent with the disclosures of the asserted prior art. In any event, even under Petitioner's broader definition, Petitioner fails to establish a reasonable likelihood of prevailing at trial with respect to any challenged claim based on the grounds of unpatentability advanced in the Petition.

C. Claim Construction

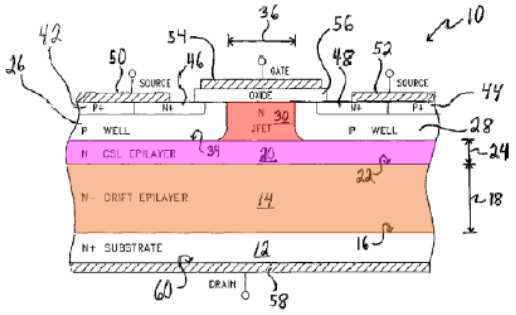
We construe claim terms only as relevant to the parties' contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid*

Techs., Inc. v. Am. Sci. & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). We agree with the parties that no claim term requires express construction for purposes of this Decision. Pet. 34–35; Prelim. Resp. 21–22. To the extent that the scope of a term requires discussion, however, we provide it in the following analysis of the challenge.

D. Analysis of the Challenge

Each independent claim specifies a current spreading semiconductor layer in relationship to a JFET region and a drift semiconductor layer. *See* Ex. 1001, 8:54–9:40, 10:20–55. As an initial matter, we observe that the plain terms of these claims specify, *inter alia*, three distinctly-claimed structures—namely, a JFET region, a current spreading layer, and a drift semiconductor layer. *Id*. The plain language of the claims describes each of those features using different wording and requires, moreover, that the JFET region is ***formed on*** the current spreading layer, which itself is ***formed on*** the drift semiconductor layer. *Id*. We limit our analysis to the dispositive question of whether Petitioner shows sufficiently that Ryu would have suggested to an ordinarily skilled artisan a device that includes a current spreading semiconductor layer as specified in the claims. *See* Pet. 40–49, 52–56 (Petitioner's information on that point).

Patent Owner argues, and we agree, that "the Petition exclusively relies on Ryu's Figure 2A embodiment to satisfy the 'current spreading semiconductor layer' limitation." Prelim. Resp. 42 (citing Pet. 40–49, 52–56); *see supra* 7 (original figure, without any annotations). We reproduce below Patent Owner's annotated illustration, which compares Figure 1 from the '633 patent with Ryu's Figure 2A.



'633 Patent Figure 1
(color added)

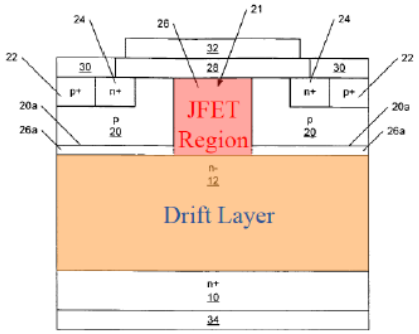
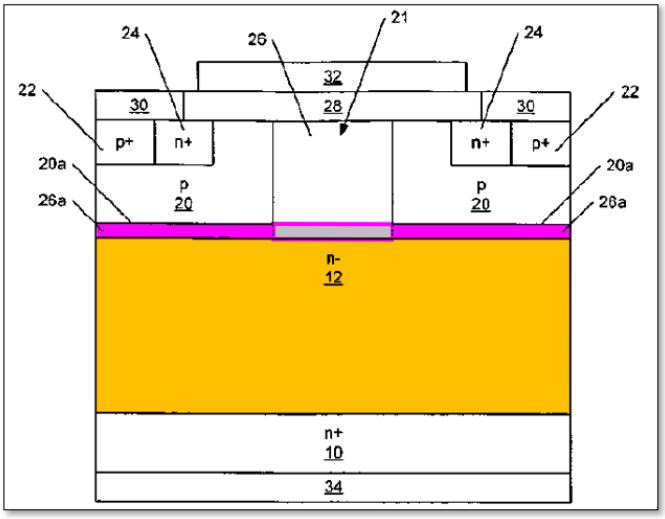


Figure 2A

Ryu Figure 2A
(annotated, color added)

Prelim. Resp. 42. The above illustration compares Figure 1 from the '633 patent, on the left, with Ryu's Figure 2A, on the right. Patent Owner annotates both figures to indicate the JFET region in salmon shading and the drift semiconductor layer in peach shading. Figure 1 from the '633 patent is annotated to show the current spreading layer in magenta shading, which finds no counterpart in Patent Owner's annotated version of Figure 2A, or the original figure, reproduced *supra* 7.

We reproduce below Petitioner's version of Ryu's Figure 2A.



EX1003, FIG. 2A (annotated)

Pet. 40; *see id*. at 40–49, 52–54 (repeatedly referring to a gray "strip" added by annotation to "JFET region 21" as a current spreading layer). Figure 2A of Ryu is a cross-sectional view of a MOSFET, which Petitioner annotates by shading magenta regions 26a in p-wells 20, shading peach drift layer 12, and by including "a strip colored grey and outlined in magenta," which, according to Petitioner, along with "regions 26a," represents "a current spreading semiconductor layer formed on a front side of the drift semiconductor layer." Pet. 40 (emphasis and text shading omitted); *see* Ex. 1003 ¶¶ 28, 42 (Ryu).

Petitioner repeatedly refers to a grey-shaded "strip" within Ryu's JFET region 21, which does not appear in Ryu's Figure 2A, but which Petitioner ***adds*** to Ryu's Figure 2A by color annotations. Pet. 40–49, 52–56; *see supra* 7 (Ryu's unannotated Figure 2A, illustrating no such "strip"). Stated somewhat differently, Petitioner argues that JFET region 21, shown in Ryu's Figure 2A, represents two distinctly-claimed structures, namely, the JFET region ***and*** the current spreading layer. Pet. 40–49, 52–56.

In Patent Owner's view, "Petitioner's argument," which attempts to establish in Ryu a disclosure of a current spreading layer, "rests entirely on [Petitioner's] own unsupported annotations of Ryu's Figure 2A." Prelim. Resp. 46. According to Patent Owner, "Petitioner cannot rely on its own annotations to create features that Ryu itself [does] not disclose." *Id*.

On that point, we agree with Patent Owner that the Board has denied review in prior cases, under similar circumstances, where a petitioner relies on its own annotations to establish structural features in figures, "where no such" features "are shown in the original figures." Prelim. Resp. 46 (quoting *Satco Prods., Inc. v. Seoul Viosys Co., LTD*, IPR2020-00655, Paper 7 at 21

(PTAB Sept. 16, 2020)); *see Fellowes, Inc. v. TreeFrog Developments, Inc.*, IPR2020-00869, Paper 18 at 7 (PTAB Feb. 24, 2021) (rejecting an attempt to divide a single prior art structure "into areas artificially generated by [p]etitioner's own annotations to" a prior art figure). In particular, we determine that Petitioner selectively shades, in grey, a portion of JFET region 21 in Ryu's Figure 2A to create a current spreading layer, where no such feature is shown in the original figure or otherwise disclosed in Ryu. Pet. 40; Ex. 1003, Fig. 2A.

Petitioner, however, further argues that an ordinarily skilled artisan "would have understood Ryu's regions 26a and the strip to be a 'current spreading layer' both because . . . current spreads laterally within it and Ryu forms that layer in the same way as the '633 patent forms its current spreading layer." Pet. 40 (text shading omitted) (citing Ex. 1035 ¶ 85). On that point, we agree with Patent Owner that this is an inherency argument. Prelim. Resp. 49; *see id*. at 53 (further distinguishing the process of Ryu from the process disclosed in the '633 patent). Inherency "is a high bar that requires the missing element be '***necessarily*** present,' not merely probably or possibly present, in the prior art." Prelim. Resp. 49 (citation omitted; Patent Owner's emphasis). Although Petitioner points out that both Ryu and the '633 patent involve p-wells that are "implanted" (Ex. 1003 ¶¶ 41–42 (Ryu)) or formed by "ion implantation" (Ex. 1001, 5:57–60), Petitioner does not explain adequately why that asserted similarity supports a conclusion that Ryu's process ***necessarily*** produces a MOSFET having a current spreading layer as claimed in the '633 patent. Pet. 48–49. Petitioner, therefore, does not meet that "high bar" in the Petition. *See* Pet. 48–49 (inadequate analysis).

In a nutshell, Petitioner does not explain adequately why an ordinarily skilled artisan would have distinguished two structural components from the single component—JFET region 21—that is illustrated in Ryu's Figure 2A. Petitioner's rationale is insufficient to support trial institution because it is not tethered adequately to any intrinsic disclosure within the four corners of the reference. Pet. 40. Petitioner relies largely on extrinsic opinion testimony and background publications. *Id*. at 43–48. We detect in this exercise the taint of impermissible hindsight reconstruction.

On this record, Petitioner fails to show sufficiently that Ryu discloses a current spreading layer as specified in the challenged claims. *Compare* Pet. 40–51*, with* Prelim. Resp. 41–53. That deficiency undermines the sole ground of unpatentability set forth in the Petition. *See* Pet. 4 (identification of challenge). Accordingly, Petitioner does not show a reasonable likelihood of prevailing at trial with respect to any challenged claim.

IV. CONCLUSION

Based on the information presented in the Petition and the Preliminary Response, we deny the Petition and do not institute an *inter partes* review.

V. ORDER

It is

ORDERED that the Petition is *denied* and no *inter partes* review is instituted.

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