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Paper 42
Entered: July 8, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS LLC, DELL TECHNOLOGIES INC., DELL INC., and HP INC.,
Petitioner,

v.

UNIFICATION TECHNOLOGIES LLC,
Patent Owner.

IPR2021-00343
Patent 8,533,406 B2

Before JUSTIN T. ARBES, TERRENCE W. McMILLIN, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges.*[1]

ARBES, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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[1] Katherine K. Vidal, Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office (Director), is recused from this proceeding and took no part in this decision. *See* Director's Memorandum, Procedures for Recusal to Avoid Conflicts of Interest and Delegations of Authority (Apr. 20, 2022) (Recusal Procedure Memo), *available at* https://go.usa.gov/xJjch; Interim Process for Director Review (§ 20), *available at* https://go.usa.gov/xJjce.

I. INTRODUCTION

A. Background and Summary

Petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., Micron Technology Texas LLC, Dell Technologies Inc., Dell Inc., and HP Inc. (collectively, "Petitioner") filed a Petition (Paper 4, "Pet.") requesting *inter partes* review of claims 15–21 and 26–30 of U.S. Patent No. 8,533,406 B2 (Ex. 1001, "the '406 patent") pursuant to 35 U.S.C. § 311(a). On July 9, 2021, we instituted an *inter partes* review as to all challenged claims on all grounds of unpatentability asserted in the Petition. Paper 9 ("Decision on Institution" or "Dec. on Inst."). Patent Owner Unification Technologies LLC subsequently filed a Patent Owner Response (Paper 21, "PO Resp."), Petitioner filed a Reply (Paper 28, "Reply"), and Patent Owner filed a Sur-Reply (Paper 33, "Sur-Reply"). An oral hearing was held on April 13, 2022, and a transcript of the hearing is included in the record (Paper 36, "Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 15–21 and 26 of the '406 patent are unpatentable, and we cannot reach a decision on the merits with respect to whether Petitioner has established the unpatentability of claims 27–30.

B. Related Matters

The parties indicate that the '406 patent is the subject of the following district court cases: *Unification Technologies LLC v. Dell Technologies, Inc.*, Case No. 6:20-cv-499-ADA (W.D. Tex.), *Unification Technologies LLC v. HP Inc.*, Case No. 6:20-cv-501-ADA (W.D. Tex.), and *Unification*

Technologies LLC v. Micron Technology, Inc., Case No. 6:20-cv-500-ADA (W.D. Tex.) ("the district court case"). Pet. 66; Paper 6, 2–3. Petitioner also filed petitions challenging claims of patents related to the '406 patent in Cases IPR2021-00344 and IPR2021-00345.

C. The '406 Patent

The '406 patent discloses techniques for "managing data in a storage device using an empty data segment directive." Ex. 1001, col. 1, ll. 28–30. "Typically, when data is no longer useful it may be erased. In many file systems, an erase command deletes a directory entry in the file system while leaving the data in place in the storage device containing the data," such that the storage device is unaware that the data is now invalid. *Id.* at col. 1, ll. 32–36. "Another method of erasing data is to write zeros, ones, or some other null data character to the data storage device to actually replace the erased file," but doing so is inefficient because "valuable bandwidth is used while transmitting the data" and "space in the storage device is taken up by the data used to overwrite invalid data." *Id.* at col. 1, ll. 36–42. The '406 patent attempts to overcome these issues by having the storage device "receive a directive that data is to be erased" and store a "data segment token" that represents erased data, rather than performing either of the typical erase methods. *Id.* at col. 1, l. 63–col. 2, l. 1.

Figure 1A of the '406 patent is reproduced below.

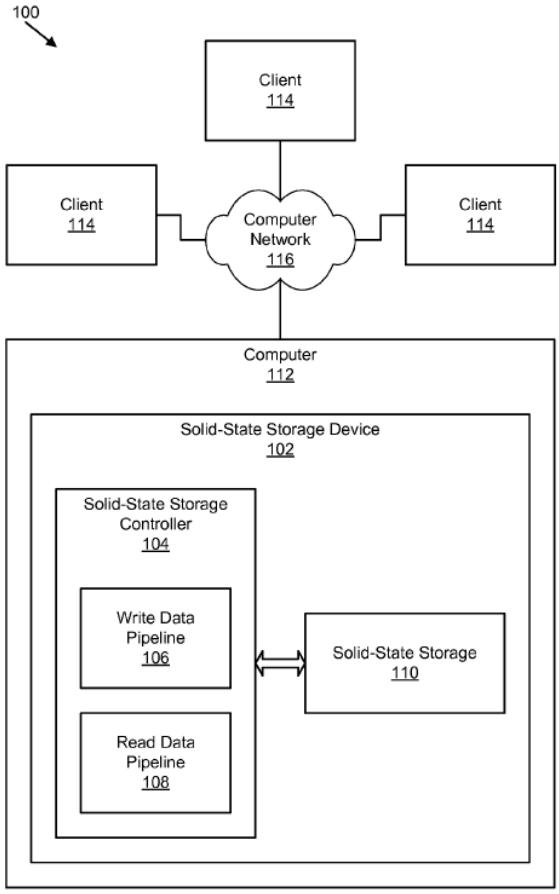

FIG. 1A

Figure 1A depicts clients 114 in communication over computer network 116 with computer 112 having solid-state storage device 102.[2] *Id.* at col. 6, ll. 44–51. Solid-state storage device 102 comprises solid-state storage 110 (e.g., flash memory) and solid-state storage controller 104 for writing to solid-state storage 110 (via write data pipeline 106), reading from solid-state storage 110 (via read data pipeline 108), and performing other operations on

[2] A solid-state storage device is a type of non-volatile memory that stores data in pages within blocks, where each page is identified by a unique physical address. Data in a solid-state storage device cannot be directly overwritten with new data, but instead must first be erased (at the block level) and then written (to pages). *See* Ex. 1001, col. 1, ll. 43–50.

solid-state storage 110. *Id.* at col. 6, ll. 52–59. When a "data packet is stored and the physical address of the data packet is assigned," the solid-state storage controller creates an entry in an index that maps a "logical identifier" of the object to "one or more physical addresses corresponding to where the storage controller" stored the data packet and any object metadata packets. *Id.* at col. 11, ll. 53–59.

Write data pipeline 106 includes garbage collector bypass 316 that "receives data segments from the read data pipeline 108 as part of a data bypass in a garbage collection system." *Id.* at col. 27, ll. 19–22, Fig. 3. According to the '406 patent,

> [a] garbage collection system typically marks packets that are no longer valid, typically because the packet is marked for deletion or has been modified and the modified data is stored in a different location. At some point, the garbage collection system determines that a particular section of storage may be recovered. This determination may be due to a lack of available storage capacity, the percentage of data marked as invalid reaching a threshold, a consolidation of valid data, an error detection rate for that section of storage reaching a threshold, or improving performance based on data distribution, etc. Numerous factors may be considered by a garbage collection algorithm to determine when a section of storage is to be recovered.

Id. at col. 27, ll. 22–34. The '406 patent discloses an apparatus comprising (1) a "request receiver module" that "receive[s] an indication identifying data that can be erased from a non-volatile storage medium," where the indication identifies the data using a "logical identifier," (2) a "marking module" that "invalidate[s] an association between the logical identifier and the physical address" to which the logical identifier is mapped in the index, (3) a "storage recovery module" that "recover[s] the physical storage location at the physical address" at an appropriate time, and (4) a "storage

module" that "store[s] data associated with another logical identifier on the physical storage location in response to recovering the physical storage location." *Id.* at col. 2, l. 61–col. 3, l. 39.

D. Illustrative Claim

Challenged claims 15, 27, and 30 of the '406 patent are independent. Claims 16–21 and 26 depend from claim 15, and claims 28 and 29 depend from claim 27. Claim 15 recites:

> 15. An apparatus, comprising:
>
> a non-volatile storage medium;
>
> a request receiver module of a storage layer for the non-volatile storage medium configured to receive an indication that a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted, wherein the indication comprises a logical identifier that is associated with the data structure by a storage client, and wherein the logical identifier is mapped to a physical address of the data on the non-volatile storage medium; and
>
> a marking module configured to record that the data stored at the physical address mapped to the logical identifier can be erased from the non-volatile storage medium in response to receiving the indication.

E. Evidence

The pending grounds of unpatentability in the instant *inter partes* review are based on the following prior art:

> U.S. Patent No. 7,624,239 B2, filed Nov. 14, 2005, issued Nov. 24, 2009 (Ex. 1002, "Bennett");
>
> U.S. Patent No. 7,057,942 B2, issued June 6, 2006 (Ex. 1003, "Suda"); and
>
> Eran Gal & Sivan Toledo, "Mapping Structures for Flash Memories: Techniques and Open Problems," *Proceedings of the*

> *IEEE International Conference on Software – Science, Technology & Engineering (SwSTE'05)*, Aug. 2005 (Ex. 1010, "SwSTE'05").

Petitioner filed a declaration from R. Jacob Baker, Ph.D., P.E. (Ex. 1004) with its Petition. Patent Owner filed a declaration from Vijay K. Madisetti, Ph.D. (Ex. 2010) with its Response. Also submitted as evidence are transcripts of the depositions of Dr. Baker (Ex. 2012) and Dr. Madisetti (Ex. 1038).

F. Asserted Grounds

This *inter partes* review involves the following grounds of unpatentability:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
15–21, 26–30	103(a)[3]	Bennett[4]

[3] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 103 and 112. Because the challenged claims of the '406 patent have an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 103 and 112. *See* Pet. 4–5.

[4] Petitioner asserts that the challenged claims are unpatentable over (1) Bennett, (2) Suda, and (3) Suda and SwSTE'05, each "in view of a [person of ordinary skill in the art's] knowledge." Pet. 8. As explained in the Decision on Institution, we do not include the general knowledge of a person of ordinary skill in the art in listing the grounds themselves, recognizing that such knowledge is considered in every obviousness analysis. *See* Dec. on Inst. 6 n.3; 35 U.S.C. § 311(b) (*inter partes* review "only on the basis of prior art consisting of patents or printed publications"); *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020) ("Although the prior art that can be considered in inter partes reviews is limited to patents and printed publications, it does not follow that we ignore the skilled artisan's knowledge when determining whether it would have been obvious to modify the prior art. . . . Regardless of the tribunal, the inquiry into whether any 'differences' between the invention and the prior

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
15–21, 26–30	103(a)	Suda
21, 26, 28	103(a)	Suda, SwSTE'05

II. ANALYSIS

A. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art for a challenged patent, we look to "1) the types of problems encountered in the art; 2) the prior art solutions to those problems; 3) the rapidity with which innovations are made; 4) the sophistication of the technology; and 5) the educational level of active workers in the field." *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 666–667 (Fed. Cir. 2000). "Not all such factors may be present in every case, and one or more of them may predominate." *Id.*

Petitioner states that it assumes an effective filing date of December 6, 2006, for the challenged claims of the '406 patent, and argues that a person of ordinary skill in the art at that time would have had "a Bachelor of Science degree in computer science or electrical engineering and at least two years of experience in the design, development, implementation, or management of solid-state memory devices." Pet. 4–5 (citing Ex. 1004 ¶ 55). According to Petitioner, an ordinarily skilled artisan also

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art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan's knowledge."); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) ("[T]he knowledge of [an ordinarily skilled] artisan is part of the store of public knowledge that must be consulted when considering whether a claimed invention would have been obvious."); *Dow Jones & Co. v. Ablaise Ltd.*, 606 F.3d 1338, 1349 (Fed. Cir. 2010) ("[The obviousness] analysis requires an assessment of the . . . 'background knowledge possessed by a person having ordinary skill in the art.'" (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007))).

> would have known, as background information: how flash memory erases data, how flash memory programs or writes data, how memory is used in a cache hierarchy, relative speeds of flash memory compared to other memory, how garbage collection is used with flash memory, how to use wear leveling to combat endurance limits of flash memory, how the [Flash Translation Layer ("FTL")] works, and industry standards affecting flash memory including the [Advance Technology Attachment ("ATA")] standard.

Id. (citing Ex. 1004 ¶¶ 55–56). Patent Owner applies the same definition of the level of ordinary skill in the art. PO Resp. 17 (citing Ex. 2010 ¶¶ 47–52). Based on the full record developed during trial, including our review of the '406 patent and the types of problems and solutions described in the '406 patent and cited prior art, we agree with Petitioner's proposed definition of the level of ordinary skill in the art and apply it for purposes of this Decision. *See, e.g.*, Ex. 1001, col. 1, ll. 25–59 (describing in the "Background of the Invention" section of the '406 patent various write, read, and erase procedures for solid-state storage devices).

B. Claim Interpretation

We interpret the claims of the challenged patent

> using the same claim construction standard that would be used to construe the [claims] in a civil action under 35 U.S.C. 282(b), including construing the [claims] in accordance with the ordinary and customary meaning of such [claims] as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2020). "In determining the meaning of [a] disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic*

Sofamor Danek, Inc., 469 F.3d 1005, 1014 (Fed. Cir. 2006). Claim terms are given their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

After the Petition was filed, the district court issued a Claim Construction Order construing various terms of the '406 patent:

Claim Term	Construction
"logical identifier"	An identifier that can be associated with a physical address on a storage device for identifying data stored at the physical address
"logical identifier [that/in the index] is empty"	Indefinite
"marking module"	Not indefinite; not subject to §112(f); plain and ordinary meaning
"storage module"	Not indefinite; not subject to §112(f); plain and ordinary meaning
"index module"	Not indefinite; not subject to §112(f); plain and ordinary meaning

Ex. 2006, 2–3.

We address three claim interpretation issues. First, in the Decision on Institution, based on the record at the time, we agreed with and adopted the district court's construction of "logical identifier." Dec. on Inst. 11–12. The parties agree with that construction. *See* PO Resp. 18; Reply 4. Based on

the full trial record, we interpret "logical identifier" in the same manner as the district court.

Second, claim 27 recites "a request receiver module configured to receive an indication comprising a logical identifier that *is empty*," and claim 30 similarly recites "a request receiver module configured to receive an indication that a specified logical identifier *is empty*" and "a read request response module configured to return an indication that the logical identifier *is empty*" (emphasis added). The district court's Claim Construction Order lists "[i]ndefinite" as the final construction for the phrase "logical identifier [that/in the index] is empty." Ex. 2006, 2 (alteration in original). Petitioner asserted in the Petition that we should instead adopt Patent Owner's original proposed construction from the district court case of "data identified by the [logical identifier] that does not need to be preserved," but Petitioner did not provide any explanation for why such an interpretation is justified. Pet. 6–7 (alteration in original). In the Decision on Institution, based on the record at the time, we explained why we were "unable to interpret the 'empty' phrases in claims 27 and 30, and c[ould]not ascertain the scope of the claims with reasonable certainty for purposes of assessing patentability." Dec. on Inst. 12–14. For example, we noted that, given the interpretation of "logical identifier" above, a logical identifier is simply "information identifying something else" and "either exists or does not exist"; it cannot be considered "empty." *Id.* at 13. We encouraged the parties, to the extent they disagreed with that determination, to "provide an explanation and cite evidence in support of the proposed interpretation in their papers during trial." *Id.* at 14.

Patent Owner argues that, based on our earlier determination, Petitioner has failed to prove that claims 27–30 are unpatentable. PO Resp. 22, 49, 53–54. Petitioner does not address claims 27–30 in its Reply.

Neither party provides any argument or evidence disputing our reasoning in the Decision on Institution or the district court's conclusion that the claim phrases are indefinite. Based on the full trial record, we maintain our earlier determination and incorporate the previous analysis herein. *See* Dec. on Inst. 12–14.

Third, with respect to the "module" terms listed above, neither party argues that the terms are means-plus-function limitations under 35 U.S.C. § 112, sixth paragraph, and the district court construed them not to be means-plus-function limitations. *See* PO Resp. 18; Reply 4; Ex. 2006, 2–3. We presume that the terms are not means-plus-function limitations because they do not use the word "means" and find no basis on the record before us to conclude otherwise. *See Dyfan, LLC v. Target Corp.*, 28 F.4th 1360, 1365 (Fed. Cir. 2022) ("Because invoking § 112 ¶ 6 is typically a choice left to the claim drafter, we presume at the first step of the analysis that a claim limitation is subject to § 112 ¶ 6 when the claim language includes the term 'means.' . . . The inverse is also true—we presume that a claim limitation is not drafted in means-plus-function format in the absence of the term 'means.' . . . [T]his presumption is rebuttable [and] can be overcome if a challenger demonstrates that the claim term 'fails to recite sufficiently definite structure.'") (citing *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348–49 (Fed. Cir. 2015)).

No other claim terms require interpretation to decide the issues presented during trial. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("Because we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy,' we need not construe [a particular claim limitation]

where the construction is not 'material to the . . . dispute.'" (citation omitted)).

C. Legal Standards

To prevail in its challenges to the patentability of claims 15–21 and 26–30 of the '406 patent, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). This burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015); *see also In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1376 (Fed. Cir. 2016) ("Where, as here, the only question presented is whether due consideration of the four *Graham* factors renders a claim or claims obvious, no burden shifts from the patent challenger to the patentee.").

A claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made." *KSR*, 550 U.S. at 406 (quoting 35 U.S.C. § 103(a) (2006)). The question of obviousness is resolved on the basis of underlying factual determinations, including "the scope and content of the prior art"; "differences between the prior art and the claims at issue"; and "the level of ordinary skill in the pertinent art." *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Additionally, objective indicia of nonobviousness, such as "commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to

the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy." *Id.* When conducting an obviousness analysis, we consider a prior art reference "not only for what it expressly teaches, but also for what it fairly suggests." *Bradium Techs. LLC v. Iancu*, 923 F.3d 1032, 1049 (Fed. Cir. 2019) (citation omitted).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418 (for an obviousness analysis, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does"). Also, "[t]hough less common, in appropriate circumstances, a patent can be obvious in light of a single prior art reference if it would have been obvious to modify that reference to arrive at the patented invention." *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016).

"Although the *KSR* test is flexible, the Board 'must still be careful not to allow hindsight reconstruction of references . . . without any explanation as to *how* or *why* the references would be combined to produce the claimed invention.'" *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016) (citation omitted). Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some

articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); *accord In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (stating that "conclusory statements" amount to an "insufficient articulation[] of motivation to combine"; "instead, the finding must be supported by a 'reasoned explanation'" (citation omitted)); *Magnum Oil*, 829 F.3d at 1380 ("To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.").

D. Obviousness Ground Based on Suda (Claims 15–21 and 26–30)

1. Suda

Suda discloses a "memory management device for managing a nonvolatile semiconductor memory." Ex. 1003, code (57). Figure 1 of Suda is reproduced below.

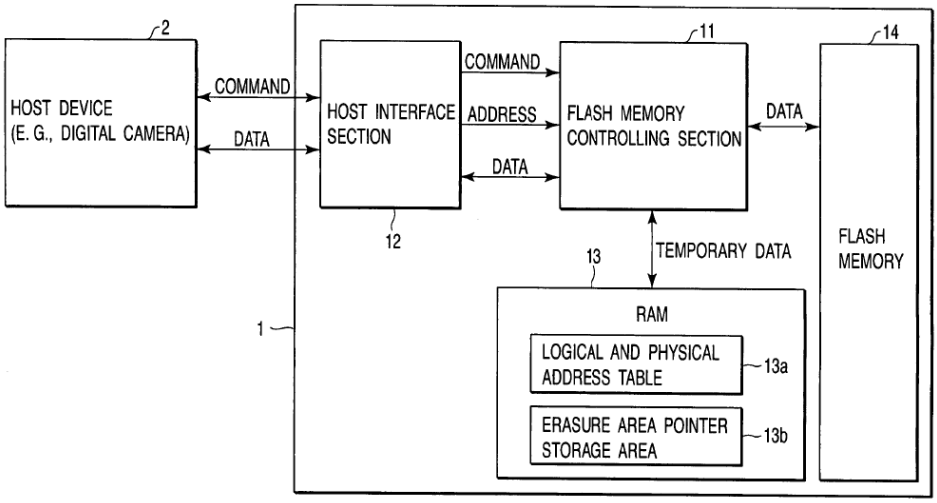

FIG. 1

Figure 1 depicts host device 2, which may be a digital camera, in communication with memory card 1 comprising host interface section 12, flash memory controlling section 11, and flash memory 14 (e.g., a NAND type nonvolatile memory). *Id.* at col. 2, ll. 58–66. "[F]lash memory controlling section 11 manages data erasure and a table indicating a relationship between logical blocks and physical blocks of the flash memory 14." *Id.* at col. 3, ll. 13–15. Logical and physical address table 13a, stored in random access memory (RAM) 13, "manages logical addresses and physical addresses allocated to physical blocks in which data items are written, of the physical blocks in the flash memory 14, in association with each other." *Id.* at col. 3, ll. 41–47.

According to Suda, when a subset of pages of a physical block are erased, "the time required for data erasure is long" because the non-erased pages must be read and "written to another physical block." *Id.* at col. 4, ll. 60–67; *see also id.* at col. 1, ll. 19–23. Suda discloses an improved process that instead writes "erasure area pointer[s]" to erasure area pointer storage area 13b in RAM 13 indicating that pages in a particular address range are in a "virtual erased state." *Id.* at col. 5, ll. 14–23. "The virtual erased state is a state in which the flash memory controlling section 11 does not actually erase data items to be erased, i.e., they are subjected to virtual erasure, in response to an access command from the host device 2." *Id.* at col. 5, ll. 23–27. Specifically, when host device 2 issues a data read command with a logical block address, flash memory controlling section 11 obtains the corresponding physical block address from logical and physical address table 13a, then looks to erasure area pointer storage area 13b to determine whether the requested data is within "an area indicated by the

erasure area pointer or pointers"; if so, flash memory controlling section 11 outputs "initial-value" (i.e., empty) data. *Id.* at col. 9, ll. 52–62.

Figure 8 of Suda is reproduced below.

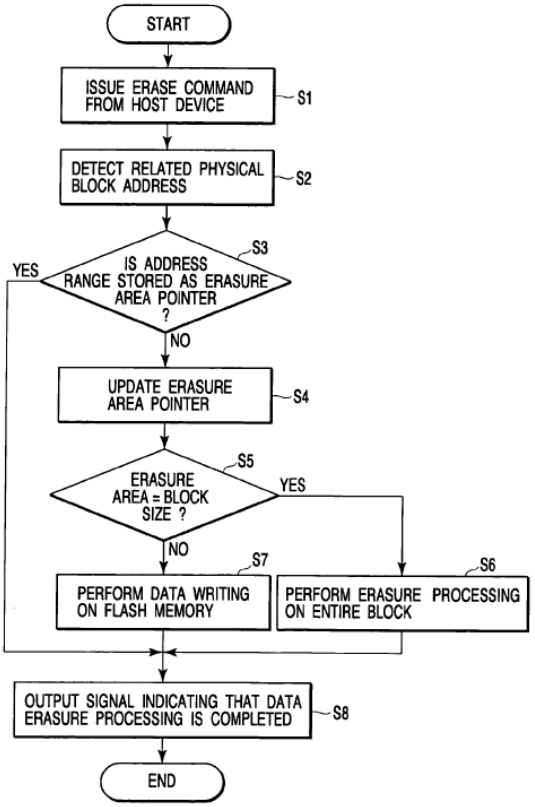

FIG. 8

Figure 8 is a flowchart depicting the disclosed erase process. *Id.* at col. 2, ll. 38–40. Host device 2 issues an erase command to erase particular pages of data stored in a physical block (step S1). *Id.* at col. 7, ll. 11–19. Flash memory controlling section 11 refers to logical and physical address table 13a and "detects the physical address of a physical block related to a logical block given an address design[at]ed in the erasure command" (step S2), then "determines whether an address range corresponding to an area in which the data items to be erased in response to the erase command are stored is already stored in the erasure area pointer storage area 13b" (step S3). *Id.* at col. 7, ll. 30–42. If not, it stores erasure area pointers (i.e., a "start pointer"

for the first page address and "end pointer" for the last page address) in erasure area pointer storage area 13b (step S4). *Id.* at col. 5, ll. 36–46, col. 7, ll. 43–55, Figs. 3–5. Flash memory controlling section 11 then "determines whether or not the address range indicated by the erasure area pointer[s] . . . is coincident with the size of a physical block to be subjected to data erasure" (step S5). *Id.* at col. 7, ll. 56–63. If it is coincident (i.e., the entire physical block is already in a "virtual erased state"), the block may be put into an "unused state" by, for example, erasing the associated address information in logical and physical address table 13a (step S6). *Id.* at col. 7, l. 64–col. 8, l. 2. If it is not coincident, flash memory controlling section 11 writes the data items written to erasure area pointer storage area 13b to flash memory 14 so that "even if a power supply to the memory card 1 is turned off, the information of the erasure area pointer is maintained, and thus a virtual erased state is also maintained" (step S7). *Id.* at col. 8, ll. 3–12.

2. Claim 15

Petitioner argues that claim 15 is unpatentable over Suda[5] under 35 U.S.C. § 103(a), relying on the testimony of Dr. Baker as support. Pet. 36–41 (citing Ex. 1004). Patent Owner makes various arguments in response, relying on the testimony of Dr. Madisetti. PO Resp. 23–38 (citing Ex. 2010); Sur-Reply 8–16.

[5] The three prior art references at issue in this proceeding (Suda, SwSTE'05, and Bennett) were not of record during prosecution of the '406 patent. *See* Ex. 1001, code (56); Pet. 9.

a) Petitioner's Arguments

Petitioner argues that Suda teaches or renders obvious all of the limitations of claim 15. Pet. 36–41. Petitioner asserts that Suda teaches an "apparatus" (i.e., the memory device shown in Figure 1) comprising a "non-volatile storage medium" (i.e., flash memory 14), "request receiver module" (i.e., host interface section 12 or flash memory controlling section 11 performing various functions in the disclosed erase process), and "marking module" (i.e., flash memory controlling section 11 performing various functions in the disclosed erase process). *Id.* Specifically, with respect to the recited "request receiver module," Petitioner argues that a person of ordinary skill in the art "would have recognized Suda's flash memory controlling section or host interface sections, both of which receive[] commands originating from a host device, as the 'request receiver module.'" *Id.* at 37–38.

Claim 15 recites that the request receiver module is configured to "receive an indication that a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted." Petitioner relies on Suda's host interface section 12 and flash memory controlling section 11 receiving an erase command from a digital camera (i.e., host device 2) connected to the memory device. *Id.* at 37–39. According to Petitioner, a person of ordinary skill in the art would have understood that the erase command from the digital camera "indicates that a digital photo (the recited 'data structure') has been selected for deletion by a user." *Id.* at 38. The digital photo "would have a data structure in the form of a .jpg, .gif, .raw, or any file system data structure" and "be stored as data on the flash memory of the memory device. Thus, a [person of ordinary skill in the art] would have understood Suda's erase command to be [an] indication that a picture file,

corresponding to digital photo data stored on the flash memory, has been deleted by a user." *Id.* (citation omitted); *see* Ex. 1003, col. 7, ll. 11–19, 34–38 (describing an example of an "erase command to erase 16384-bytes data items (32 pages) of the data items which are managed when they are stored in a physical block given physical block address '3' which is related to logical block address '0x40000' by the logical and physical address table 13a"), Fig. 7.

Claim 15 further recites that "the indication comprises a logical identifier that is associated with the data structure by a storage client" and is "mapped to a physical address of the data on the non-volatile storage medium." Petitioner argues that the erase command in Suda designates a logical block address, which constitutes a "logical identifier" and is mapped to physical block numbers in logical and physical address table 13a. Pet. 38–40 (citing Ex. 1003, col. 3, ll. 42–55, col. 7, ll. 11–18, 30–34, col. 8, l. 66–col. 9, l. 3, Fig. 7).

Finally, claim 15 recites that the marking module is configured to "record that the data stored at the physical address mapped to the logical identifier can be erased from the non-volatile storage medium in response to receiving the indication." Petitioner asserts that the erasure area pointers in Suda record that the range of data in the identified physical block is in a "virtual erased state" and can be erased later from the flash memory. *Id.* at 14–15, 40–41.

Petitioner provides the following annotated version of Figure 7 of Suda. *Id.* at 40.

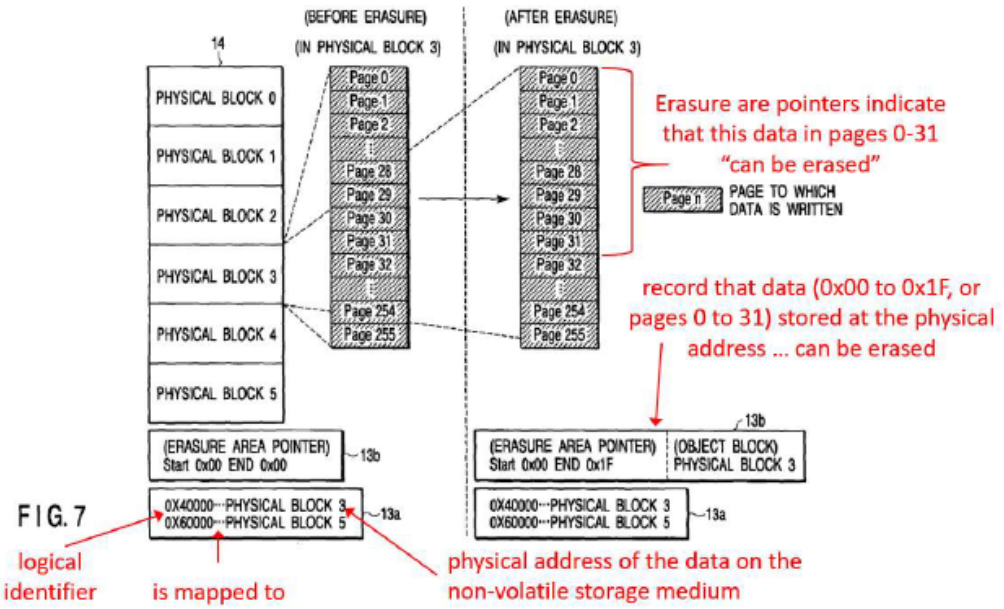

Figure 7, with Petitioner's annotations in red, depicts erasure area pointer storage area 13b before and after the entry of erasure area pointers for pages 0 to 31 of physical block 3. *Id.*; *see* Ex. 1003, col. 7, ll. 5–55. Petitioner argues that "[t]he system will physically erase a block once it fills up with virtually erased data, returning the block to an unused state." Pet. 14.

b) Patent Owner's Arguments

Patent Owner makes two arguments regarding claim 15. *See* PO Resp. 23–38; Sur-Reply 8–16. We address those arguments below.

(1) "Request Receiver Module"

First, Patent Owner disputes Petitioner's contentions regarding the recited "request receiver module." PO Resp. 23–29 (citing Ex. 2010 ¶¶ 83–90); Sur-Reply 8–13. Patent Owner argues that Petitioner identifies

two different "request receiver module[s]" (i.e., host interface section 12 and flash memory controlling section 11) receiving two different "indication[s]" (i.e., the erase command sent to host interface section 12, which Patent Owner refers to as the "Initial Command" or "Initial Message," and the command sent to flash memory controlling section 11, which Patent Owner refers to as the "Backend Command" or "Backend Instruction"), neither of which satisfies the language of the claim. PO Resp. 23–29. Patent Owner provides the following annotated version of Figure 1 of Suda. *Id.* at 26.

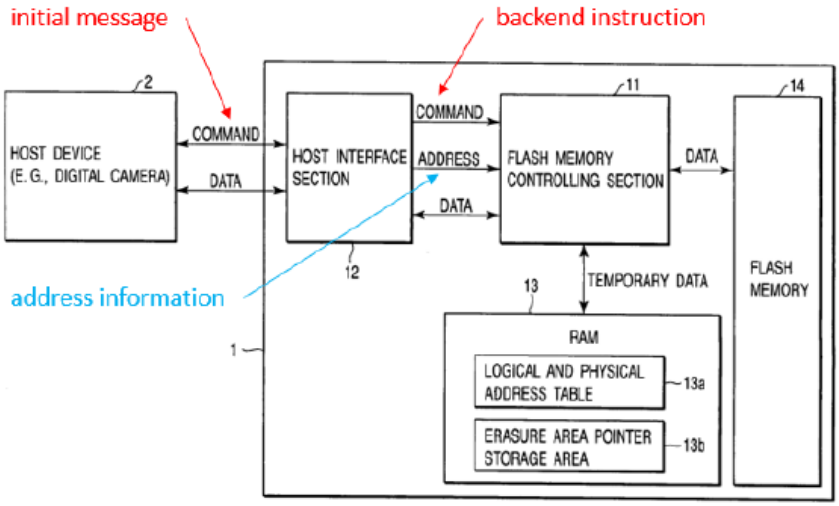

FIG. 1

Annotated Figure 1 depicts the alleged "Initial Message" (red) received by host interface section 12, and the alleged "Backend Instruction" (red) and "address information" (blue) received by flash memory controlling section 11. *Id.*

With respect to Petitioner's theory that host interface section 12 is a "request receiver module," Patent Owner argues that claim 15 recites that the marking module records data "in response to receiving the indication," but "no data is recorded in response to the Initial Message (the alleged indication)." *Id.* at 29–30; Sur-Reply 9–10. According to Patent Owner,

even though "Suda uses the words 'in response to,'" a person of ordinary skill in the art would have understood that flash memory controlling section 11 stores data in response to a different message (the Backend Command) sent by host interface section 12, not in response to the Initial Message, which "never reaches" flash memory controlling section 11. *Id.*

With respect to Petitioner's theory that flash memory controlling section 11 is a "request receiver module," Patent Owner argues that host interface section 12 extracts address information from the Initial Command and sends flash memory controlling section 11 the Backend Instruction separately from the address information over "separate buses." PO Resp. 25–28 (citing Ex. 1003, col. 3, ll. 7–9, Fig. 1); Sur-Reply 10–11. Thus, "[b]ecause the Backend Instruction does not include address information," flash memory controlling section 11 does not "receive an indication" comprising a "logical identifier" as recited in the claim. PO Resp. 28–29.

We find that host interface section 12 is a "request receiver module" that receives an "indication" comprising a "logical identifier," as recited in claim 15. Suda discloses that the erase command, which "designate[s]" a logical block address, is "issued" by host device 2 to host interface section 12. Ex. 1003, col. 3, ll. 4–6, col. 4, ll. 18–26, col. 7, ll. 11–19, 30–35, col. 8, l. 66–col. 9, l. 3. The logical block address is mapped to physical block numbers in logical and physical address table 13a, such that the logical block address is "related" to a physical block address. *Id.* at col. 7, ll. 11–19, 30–35. The logical block address designated in the erase command is a "logical identifier," given the undisputed interpretation of the term specified above. *See supra* Section II.B. Indeed, Patent Owner acknowledges that the erase command in Suda "comprises address information" and is "receiv[ed]" by host interface section 12. *See* PO Resp. 24, 28; Sur-Reply 9; Ex. 2010

¶¶ 83–84, 87. That is all the claim requires of the "request receiver module." Claim 15 imposes no requirements on what is done with the indication after it is received (apart from the marking module recording, "in response to receiving the indication," that data corresponding to the logical identifier can be erased, which we address below). *See* Sur-Reply 12 n.3. Thus, the fact that host interface section 12 extracts command and address information from the erase command and sends such information to flash memory controlling section 11 after the erase command is received is immaterial. *See* Ex. 1003, col. 3, ll. 7–9.

To the extent Patent Owner's arguments are premised on the functionality of the "marking module" recited later in claim 15, the claim only recites that the module is configured to "record that the data stored at the physical address mapped to the logical identifier can be erased from the non-volatile storage medium in response to receiving the indication." Claim 15 does not recite that the marking module itself receives the indication. To the contrary, the preceding limitation clearly recites that the request receiver module is what is "configured to receive an indication." We see nothing improper about Petitioner mapping host interface section 12 to the "request receiver module" that receives an "indication" and mapping flash memory controlling section 11 to the "marking module" that records information in response to host interface section 12 receiving the indication.

We further find that Suda teaches recording that data stored at a physical address mapped to the logical identifier can be erased "in response to receiving the indication." The processing at steps S2–S8 of Figure 8 only takes place once host interface section 12 receives the erase command from host device 2 at step S1. *See id.* at col. 7, l. 11–col. 8, l. 20. Suda states numerous times that flash memory controlling section 11 stores erasure area

pointers for a particular physical block "in response to" the erase command being received. *Id.* at col. 1, l. 60–col. 2, l. 8 ("a setting unit configured to set an address range of data to be erased *in response to* an erase command in a block in which the data to be erased is written" (emphasis added)), col. 5, ll. 38–46 ("flash memory controlling section 11 designates as a start pointer a page address . . . *in response to* an erase command from the host device 2" then "designates as an end pointer a page address" (emphasis added)), col. 6, ll. 60–63 ("erasure area pointer storage area 13b stores the data items of a physical block in which data items to be erased *in response to* an erase command from the host device 2 are stored") (emphasis added)), col. 7, ll. 11–19 ("when the host device 2 issues an erase command, . . . the processing is performed *in response to* the erase command" (emphasis added)), 43–53 ("flash memory controlling section 11 performs rewriting processing to change data written to the erasure area pointer storage area 13b . . . in order that the area in which the data items to be erased *in response to* the erase command are stored" (emphasis added)). Given these express disclosures, we disagree with Patent Owner's position that flash memory controlling section 11 records data in response to the Backend Command rather than the Initial Message (i.e., the erase command).[6] *See* PO Resp. 29–30; Sur-Reply 9–10.

[6] Patent Owner argued during the hearing that Suda does not set erasure area pointers "directly" in response to an erase command. *See* Tr. 65:1–4, 71:19–72:15. Claim 15, however, only recites recording "in response to receiving the indication." Patent Owner has not proposed an interpretation of the claim language or otherwise explained why it would be proper to add a "directly" requirement to the claim, and we see no basis on the record before us to do so. *See* Dec. on Inst. 23–24.

We are persuaded by Petitioner's arguments, supported by the testimony of Dr. Baker, which we credit, mapping host interface section 12 to the "request receiver module" and mapping flash memory controlling section 11 to the "marking module" of claim 15. *See* Pet. 37–41; Reply 10–11; Ex. 1004 ¶¶ 208–219.

Regardless, though, even if host interface section 12 alone could not be considered a "request receiver module," we also are persuaded by Petitioner's argument regarding the combination of host interface section 12 and flash memory controlling section 11. *See* Pet. 37–38 (arguing that a person of ordinary skill in the art "would have recognized Suda's flash memory controlling section or host interface sections, *both* of which receive[] commands originating from a host device, as the 'request receiver module'" (emphasis added)); Reply 10–11. We see no reason why the "request receiver module" recited in the claim cannot comprise more than one component. Indeed, Patent Owner proposed in the district court case that the term "module" should be construed to mean "a hardware circuit and/or programmable hardware and/or software implemented within a storage controller," and acknowledged during the hearing that it is not advocating a different interpretation in this proceeding. *See* Ex. 2007, 16; Tr. 56:20–57:3; Ex. 1001, col. 5, ll. 28–61 (describing "modules" broadly as implementable in, for example, "programmable hardware devices" or "software for execution by various types of processors").

Suda does not disclose explicitly what host interface section 12 and flash memory controlling section 11 are, but describes what functions they perform in the disclosed memory management device. Host interface section 12 receives commands from host device 2, "extracts" information from the received commands, and sends command and address information

to flash memory controlling section 11. Ex. 1003, col. 3, ll. 4–9. Flash memory controlling section 11 is "connected to the host device 2 by the host interface section 12" and "connected to a RAM 13 and the flash memory 14." *Id.* at col. 2, l. 66–col. 3, l. 3. It "operates based on" the information received from host interface section 12 and "manages data erasure" using tables 13a and 13b stored in RAM 13. *Id.* at col. 3, ll. 9–15. Under Petitioner's alternative theory, the combined portions (i.e., hardware and/or software) of host interface section 12 and flash memory controlling section 11 responsible for receiving and processing an erase command would qualify as a "request receiver module," and the portions of flash memory controlling section 11 responsible for recording erasure information in tables 13a and 13b would qualify as a "marking module." Contrary to Patent Owner's argument, they are not the same. *See* Sur-Reply 11–12.

For the reasons explained above, we find that host interface section 12 alone, or, alternatively, the combined portions of host interface section 12 and flash memory controlling section 11 described above, constitute a "request receiver module" receiving an "indication" comprising a "logical identifier," as recited in claim 15.[7]

(2) "Indication"

Second, Patent Owner argues that Suda does not teach or suggest receiving "an indication that a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted," as recited in claim 15. PO Resp. 30–38 (citing Ex. 2010 ¶¶ 91–103); Sur-Reply 13–16. Patent

[7] Accordingly, we need not address Petitioner's other argument that flash memory controlling section 11 alone is a "request receiver module."

Owner contends that the perspective of the user of the digital camera "is irrelevant to whether a data structure has been deleted." PO Resp. 36–38. Patent Owner disputes Petitioner's and Dr. Baker's view that the erase command indicates that the user selected a digital photo (stored as a particular type of data structure, such as a .jpg) for deletion, arguing that Suda does not use the word "photo" or disclose erasing a digital photo in the manner described by Dr. Baker. *Id.* at 30–32. Petitioner's reading of Suda also is incorrect according to Patent Owner because a "storage medium data structure refers to a data structure used by the storage medium," the "file extension of a digital photo (e.g., .jpg, .gif, etc.) is not a storage medium data structure," and "file extensions of the underlying data are meaningless to the storage system" because "[t]he storage system simply stores data." *Id.* at 35–36 (quoting Ex. 2010 ¶ 100).

As an initial matter, we disagree with Patent Owner's view that the perspective of the digital camera user is irrelevant. Claim 15 does not explicitly state from what perspective the data structure "has been deleted," and thus does not expressly preclude the deletion being assessed from the perspective of the host device sending the indication. Petitioner's understanding, though, is the most natural reading of the claim. Claim 15 recites an apparatus with a request receiver module that "receive[s] an indication that a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted." In response to the receiving of that indication, the marking module of the apparatus records that the data stored at the relevant physical address "can be erased from the non-volatile storage medium." Thus, the data on the non-volatile storage medium has not been "erased" yet when the indication is received, but the received indication indicates that a data structure corresponding to that data has been

"deleted." This is consistent with Petitioner's view of Suda, where the data on flash memory 14 has not been erased at the time the erase command is received, but the erase command indicates that a data structure corresponding to that data has been deleted. *See* Pet. 37–41.

What we must determine is how a person of ordinary skill in the art would have understood Suda's disclosure—namely, whether a person of ordinary skill in the art would have understood Suda's erase command to indicate that "a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted." *See Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1336 (Fed. Cir. 2008) ("[T]he meaning of a prior art reference requires analysis of the understanding of an artisan of ordinary skill."). In doing so, we consider the testimony of the parties' experts, who have different views. *See Acoustic Tech., Inc. v. Itron Networked Solutions, Inc.*, 949 F.3d 1366, 1373 (Fed. Cir. 2020) ("Expert testimony may shed light on what a skilled artisan would reasonably understand or infer from a prior art reference.").

Suda discloses a digital camera as a host device that uses flash memory to store data. Ex. 1003, col. 2, l. 58–col. 3, l. 15, Fig. 1. The digital camera "issues an erase command to erase" particular pages of data stored in the flash memory (identified by the provided logical block address), causing flash memory controlling section 11 to perform the disclosed erase process. *Id.* at col. 7, ll. 11–19, col. 8, l. 66–col. 9, l. 3. Suda teaches a specific type of host device (i.e., a digital camera) that was known to store specific types of files (e.g., .jpg, .gif, .raw image files) in memory and that sent a command to the memory card to erase data stored on the flash memory. *See* Ex. 1004 ¶ 211.

A person of ordinary skill in the art reading Suda would have understood the way in which file systems delete host data when sending an "erase command" to flash memory. *See Fleming v. Cirrus Design Corp.*, 28 F.4th 1214, 1223 (Fed. Cir. 2022) ("Since *KSR*, we have explained that it is appropriate to consider the knowledge, creativity, and common sense of a skilled artisan in an obviousness determination."); *supra* Section II.A (the parties' agreed definition of the level of ordinary skill in the art includes knowledge of "how flash memory erases data, how flash memory programs or writes data, how memory is used in a cache hierarchy," etc.); Ex. 1004 ¶¶ 83–89. Dr. Baker describes the "chain of events when a user reads, writes, or deletes data in a computer system with flash memory" as follows:

> A user interacts, through a user interface, with an application or an operating system to modify certain data. For example, the user may specify a file name (e.g., "C:\document.doc") to be read/written/deleted. Operating systems then access a "file" that translates the file name into another logical address (e.g., a file indicating that "C:\document.doc" is stored at logical address 0x4000). The operating system then generates a command to read, write, or delete data stored at a logical identifier (e.g., at the logical address, or at the file name). The driver and the file system then work together to convert the operating system's command into the specific electrical signals understood by the flash memory device in order to read, write, or delete data on the flash drive. As part of this process, some file system data in RAM may be modified, and a modification to corresponding file system data on the flash drive will be performed. For example, when sending erase commands, the computer updates its own system "file" in RAM to indicate that C:\document.doc is erased and no longer stored at logical address 0x4000, such as by erasing this file entry.

Ex. 1004 ¶ 89. The device receiving the erase command would "then operate as described" in Suda. *Id.* This is consistent with the '406 patent itself, which states in the "Background of the Invention" section that

"[t]ypically, when data is no longer useful it may be erased. In many file systems, an erase command deletes a directory entry in the file system while leaving the data in place in the storage device containing the data." *See* Ex. 1001, col. 1, ll. 25–35; *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022) ("[A] patentee's admissions about the scope and content of the prior art provide a factual foundation as to what a skilled artisan would have known at the time of invention."); *Koninklijke Philips*, 948 F.3d at 1337; *Randall Mfg.*, 733 F.3d at 1362. We find Dr. Baker's analysis persuasive as to how an ordinarily skilled artisan would have understood Suda's description of an "erase command" sent by the digital camera.

Dr. Baker's view also is consistent with Suda's description of what happens after the erase command. In particular, in response to the erase command, flash memory controlling section 11 sets erasure area pointers in erasure area pointer storage area 13b, which prevents the data from being read. *See* Ex. 1003, col. 8, ll. 24–38 (disclosing that when a read request is submitted, flash memory controlling section 11 outputs "initial-value data" if the applicable page range is "included in the area indicated by the erasure area pointer"). Thus, "the photo is deleted from the user's point of view (i.e., the camera's / camera software's point of view) and cannot be read." Reply 12. Based on our review of the full trial record, we find that Dr. Baker's explanation as to what a person of ordinary skill in the art allegedly would have understood the erase command to indicate to the flash memory controlling section in the digital camera embodiment is most consistent with the disclosure of Suda. *See* Pet. 37–39; Ex. 1004 ¶ 211. We are persuaded that a person of ordinary skill in the art would have read the reference in the manner he describes. *See id.*

Finally, we disagree with Patent Owner's arguments regarding file extensions. *See* PO Resp. 35–36; Sur-Reply 15–16. The indication in claim 15 is that a "data structure" (not a "storage medium data structure" as Patent Owner states) "corresponding to data stored on the non-volatile storage medium, has been deleted." For the reasons explained above, we agree with Petitioner and Dr. Baker that a person of ordinary skill in the art would have understood Suda to mean that a data structure for a digital photo selected by the user has been deleted when the digital camera sends an erase command. *See* Pet. 38–39; Reply 13; Ex. 1004 ¶ 89. After reviewing the full trial record, we find that Petitioner has made a sufficient showing regarding the "indication" of claim 15.[8]

Patent Owner also makes various other arguments regarding Suda's disclosure in column 5 of "canceling the relation between the logical block addresses and the physical block addresses." PO Resp. 32–33 (quoting Ex. 1003, col. 5, ll. 65–67). Patent Owner contends that even after canceling the relation in Suda, "the specific logical address would still be usable." *Id.* According to Patent Owner, Figures 8 and 9 also "do not describe the erase command as removing a mapping between a logical address and a physical address." *Id.* at 33. With respect to Figure 8, step S3 "confirms that the

[8] To the extent Petitioner relies on Patent Owner's infringement contentions in the district court case (Ex. 1013) for the purpose of either showing that Suda's logical block address is a "logical identifier" (Pet. 38) or that Suda teaches a similar "indication" to what Patent Owner accuses of infringement (Reply 13), we are not persuaded. Petitioner does not explain, and we do not see, how Patent Owner's arguments regarding alleged infringement by Petitioner's products are relevant to our inquiry here: determining whether Suda teaches or suggests the recited "indication." *See* Dec. on Inst. 32–33; Sur-Reply 13–14. We give no weight to the infringement contentions in conducting that analysis.

physical address corresponding to the logical address provided in the erase command was not previously marked for erasure," but if the erase command removed the mapping, "it would not be possible for a physical address to be previously marked for erasure." *Id.* at 33–34. With respect to Figure 9, step A2 similarly confirms whether the "physical address corresponding to the logical address provided in the read command was not previously marked for erasure," which "means that even after processing an erase command, a logical address can refer to a physical address that was marked for erasure." *Id.* at 34–36.

Petitioner, however, does not rely on Suda's column 5 disclosure of canceling a relation between a logical block address and physical address for purposes of claim 15. *See* Pet. 37–41. Petitioner's position with respect to claim 15 is that the erase command sent by the digital camera indicates that a data structure has been deleted, the erase command includes a logical block address corresponding to the physical address where the digital photo is stored in the flash memory, and, in response to the erase command, flash memory controlling section 11 sets erasure area pointers in erasure area pointer storage area 13b so that the data at the corresponding physical address "can be erased" at some point in the future. *Id.* We find that analysis persuasive for the reasons explained above, and address the parties' arguments regarding Suda's other disclosures below when addressing dependent claims 16 and 17. *See infra* Sections II.D.3–4.

c) Conclusion

Petitioner has shown sufficiently that a person of ordinary skill in the art would have understood Suda to teach all of the limitations of claim 15. *See* Pet. 36–41; Ex. 1004 ¶¶ 204–219. Petitioner has proven, by a

preponderance of the evidence, that claim 15 would have been obvious based on Suda under 35 U.S.C. § 103(a).

3. Claim 16

Claim 16 depends from claim 15 and recites that "the marking module is configured to record that data stored at a physical address on the non-volatile storage medium can be erased from the non-volatile storage medium by invalidating an association between the logical identifier and the physical address." Petitioner argues that a person of ordinary skill in the art would have understood that "canceling the relation between the logical block addresses and the physical addresses" (in the example of Figure 4, described in column 5 of Suda) and "eras[ing] address information" (in the example of Figure 6, physical block B, described in column 6 of Suda) both constitute "invalidating an association" between a logical identifier and physical address. Pet. 41–42 (quoting Ex. 1003, col. 5, l. 65–col. 6, l. 3, col. 6, ll. 35–41; citing Ex. 1004 ¶ 222). "In these scenarios, an erase command is received to delete at least an entire block." *Id.* at 41 (citing Ex. 1003, col. 6, ll. 15–21).

Patent Owner responds that Suda does not teach "invalidating an association between the logical identifier and the physical address." PO Resp. 38–42 (citing Ex. 2010 ¶¶ 104–106); Sur-Reply 16–19. Patent Owner argues that Suda does not use the word "invalid" at all and in fact "suggests the opposite" of invalidation because it "discloses checking to make sure that the physical addresses associated with both erase commands and read commands do not fall within an erasure area," citing Suda's description of Figures 8 and 9. PO Resp. 38. As to Figure 8 depicting an erase process, Patent Owner contends that prior to performing steps S4–S7,

Suda in step S3 "check[s] to see if 'data items to be erased in response to the erase command' are 'already stored in the erasure area pointer storage area.'" *Id.* at 38–39 (quoting Ex. 1003, col. 7, ll. 38–42). As to Figure 9 depicting a read process, Patent Owner contends that Suda likewise "refers to the erasure area pointer storage area 13b, and determines whether a page range in which data items to be read is included in the area indicated by the erasure area pointer." *Id.* at 39–40 (quoting Ex. 1003, col. 8, ll. 30–34). According to Patent Owner and Dr. Madisetti, "[t]he fact that Suda recognizes erase and read requests can involve physical addresses that are within the erasure area pointer, means that the purported cancellation does not invalidate the association between the logical identifier and the physical address." *Id.* at 40 (quoting Ex. 2010 ¶ 105). Patent Owner reasons that

> [i]f the virtual erase state invalidated an association between the logical identifier and the physical address, that would mean that logical addresses would no longer map to the physical address containing the invalid data. Suda's disclosure that the physical block address must be checked against the erasure area pointers in read and erase requests means that Suda does not disclose or render obvious invalidating an association between the logical identifier and the physical address. Indeed, if cancellation amounted to invalidation, it would not be necessary for either erase or read requests to confirm the requested materials are outside the erasure area pointers.

Id. at 41 (quoting Ex. 2010 ¶ 105); Sur-Reply 16.

Finally, Patent Owner points out that the portions of Suda relied upon by Petitioner for the alleged "indication" (i.e., erase command) with respect to parent claim 15 are "different from the erasure area pointers section of Suda that discloses cancelling the relation between logical and physical addresses" with respect to dependent claim 16, and the alleged invalidation

is not "in response to receiving the indication." PO Resp. 41–42; Sur-Reply 18–19.

After reviewing the full trial record, we find that a person of ordinary skill in the art would have understood that Suda's description of "eras[ing] address information" in the example of Figure 6 constitutes "invalidating an association" between a logical identifier and physical address, as recited in claim 16.[9] Figure 6 of Suda is reproduced below.

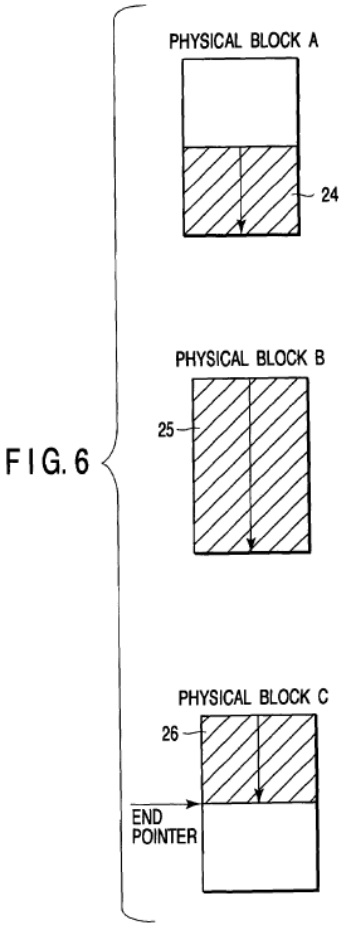

FIG. 6

[9] Because we find Petitioner's showing with respect to "eras[ing] address information" in Suda sufficient, we need not address whether Suda's other description of "canceling the relation between the logical block addresses and the physical addresses" likewise constitutes "invalidating an association" between a logical identifier and physical address. *See* Pet. 41–42.

Figure 6 depicts exemplary uses of erasure area pointers to denote virtual erasure areas of physical blocks. Ex. 1003, col. 6, ll. 15–16. Suda provides

> an explanation of processing in the case where *an erase command* to erase data items written to a number of physical blocks in the flash memory 14 *is issued from the host device 2*.
>
> To be more specific, the processing will be explained by referring to the case where *an erase command* to erase data items written to three physical blocks (physical blocks A, B and C) *is issued from the host device 2*. . . .
>
> With respect to the physical block B, the data items written to the entire area of the physical block B are to be erased. Thus, the flash memory controlling section 11 . . . *erases address information of the physical block B and a logical block address related to the address information of the physical block B from the logical and physical address table 13a*, thereby setting the entire area (area 25) of the physical block B in an unused state.

Id. at col. 6, ll. 18–41 (emphasis added). The scenario described with respect to physical block B occurs when the full block contains data to be virtually erased (unlike, for example, physical blocks A and C where only part of the physical block is to be virtually erased). *See id.* at col. 6, ll. 34–36; Pet. 14 ("When erasing the block, the corresponding logical and physical address entry is removed."), 41–42 ("[A]n erase command is received to delete at least an entire block."); Ex. 1004 ¶¶ 221–222.

Erasing address information from logical and physical address table 13a reflecting the association between a logical block address and physical block address in Suda constitutes "invalidating an association between the logical identifier and the physical address." *See* Pet. 41–42. It also is performed "in response to receiving the indication." The excerpt of Suda quoted above discloses that the processing begins with the erase command to erase data items written to physical block B being issued from host device 2;

address information is erased in response to that command, returning the full physical block to an unused state.[10] *See* Ex. 1003, col. 6, ll. 18–41.

We also disagree with Patent Owner's arguments regarding Figures 8 and 9. Figure 8 depicts a "procedure for erasing data written to the memory card 1," and Figure 9 depicts a "procedure for reading data written to the memory card 1," in Suda's "second example." *Id.* at col. 2, ll. 38–43. Both, therefore, assume that there is "data written to the memory card 1." *See id.* In other words, there is a valid mapping to data written in physical blocks. Indeed, Suda discloses that for Figure 8, "the structures of physical blocks not yet subjected to data erasure and the contents of information to be managed by the logical and physical address table 13a are the same as those in the first example" (i.e., Figure 2, showing two entries in logical and physical address table 13a), suggesting that Figure 8 is not describing the scenario of Figure 6 (physical block B) where address information has been removed from logical and physical address table 13a. *See id.* at col. 3, ll. 16–19, col. 7, ll. 19–25. Also, step S2 of Figure 8 and step A1 of Figure 9 both involve detecting a physical block address related to a logical block

[10] We recognize that Petitioner's contentions for claims 15 and 16 are different, as Patent Owner points out. *See* PO Resp. 41–42; Sur-Reply 18–19. Claim 15 recites "record[ing] that the data stored at the physical address mapped to the logical identifier can be erased from the non-volatile storage medium," and Petitioner relies on the setting of erasure area pointers in erasure area pointer storage area 13b. Pet. 40–41. Dependent claim 16 recites that the recording is performed "by" invalidating an association between the logical identifier and physical address, and Petitioner relies on the erasing of address information in logical and physical address table 13a (when a full physical block is to be erased). *Id.* at 41–42. We see no inconsistency in that analysis, as claim 16 simply narrows the broader scope of claim 15 by specifying the exact manner in which the recording is performed.

address in logical and physical address table 13a. *Id.* at col. 7, ll. 30–35, col. 8, ll. 24–30. Logically, therefore, the scenario described in reference to Figures 8 and 9 would "occur[] when data in only a part of a block was subjected to an erase command, causing erasure area pointers to mark that part of the block invalid, without invalidating the address mappings" (like what would occur for a full physical block, as described in reference to physical block B of Figure 6). *See* Reply 15.

We find that Suda teaches "invalidating an association between the logical identifier and the physical address," for the reasons stated by Petitioner. *See* Pet. 41–42; Ex. 1004 ¶¶ 220–223. Petitioner has proven, by a preponderance of the evidence, that claim 16 would have been obvious based on Suda under 35 U.S.C. § 103(a).

4. Claim 17

Claim 17 depends from claim 15 and recites that "the marking module is configured to record that data stored at a physical address on the non-volatile storage medium can be erased from the non-volatile storage medium by deleting a mapping between the logical identifier and the physical address." Petitioner argues that a person of ordinary skill in the art would have understood Suda's description of the examples in Figures 4 and 6 to constitute deleting a mapping as recited, "for cases where at least an entire block is being deleted." Pet. 42–43 (citing Ex. 1003, col. 5, l. 65–col. 6, l. 3, col. 6, ll. 35–41; Ex. 1004 ¶¶ 224–226).

Patent Owner responds that the cited disclosures from Suda do not teach "deleting a mapping between the logical identifier and the physical address," making substantially the same arguments regarding Figures 8 and 9 as those made with respect to claim 16. *Compare* PO Resp. 38–42, *with*

id. at 43–46; *compare* Ex. 2010 ¶¶ 104–106, *with id.* ¶¶ 107–109. We disagree for the reasons explained above. *See supra* Section II.D.3. Patent Owner also acknowledges that Suda's column 6 disclosure of erasing address information reflecting the association between a logical block address and physical address "does describe deleting a mapping." Tr. 67:6–68:10; *see* Ex. 1003, col. 6, ll. 35–41. And Patent Owner and Dr. Madisetti acknowledge that Suda's column 5 disclosure of canceling a relation between a logical block address and physical address "removes the mapping between a logical and physical address." *See* PO Resp. 32 (citing Ex. 1003, col. 5, ll. 65–67); Ex. 2010 ¶ 95 (same). Thus, we find that Suda teaches "deleting a mapping between the logical identifier and the physical address." *See* Pet. 42–43; Ex. 1004 ¶¶ 224–226.

Petitioner has proven, by a preponderance of the evidence, that claim 17 would have been obvious based on Suda under 35 U.S.C. § 103(a).

5. Claims 18–20

Claim 18 depends from claim 15 and recites "an index comprising mappings between logical identifiers and physical addresses on the non-volatile storage medium, wherein the marking module is configured to remove a mapping between the logical identifier and the physical addresses of the data from the index." Petitioner argues that "Suda's controller maintains a logical and physical address table as part of an index of mappings between logical addresses . . . and physical addresses," and, for the "remove a mapping" limitation in claim 18, relies on Petitioner's earlier analysis of "deleting a mapping" in claim 17. Pet. 43.

Claim 19 depends from claim 18 and recites that "the marking module is configured to delete a reference to the physical address from an index

entry of the logical identifier." Petitioner again points to Suda's teachings of canceling the relation between the logical block address and physical address, and erasing address information from logical and physical address table 13a. *Id.* at 43–44.

Claim 20 depends from claim 18 and recites that "removal of the mapping indicates that data stored at the physical address can be erased from the non-volatile storage medium." Petitioner argues, for example, that canceling the relation between the logical block address and physical address in Suda is performed to set the physical block in an "unused state," which "means that the cancellation is performed to indicate that the block (including the data therein) can and will be erased." *Id.* at 44–45.

Patent Owner does not argue separately dependent claims 18–20. *See* PO Resp. 23–49; Sur-Reply 8–20. We disagree with Patent Owner's arguments regarding parent claim 15 and dependent claim 17 for the reasons explained above. *See supra* Sections II.D.2, II.D.4. We have reviewed Petitioner's contentions and supporting evidence, including the testimony of Dr. Baker, and are persuaded that Petitioner has proven, by a preponderance of the evidence, that claims 18–20 would have been obvious based on Suda under 35 U.S.C. § 103(a), for the reasons stated by Petitioner. *See* Pet. 43–45; Ex. 1004 ¶¶ 227–232.

6. Claim 21

Claim 21 depends from claim 15 and recites that "the marking module is configured to mark a data packet at the physical address invalid." Petitioner argues that Suda stores "'erasure area pointers' to mark data packets at a physical address as in a 'virtual erased state,'" where "[v]irtual erased data is 'subjected to virtual erasure' and can no longer be read by a

user because the system will return initial-value (empty) data instead of the actual data stored therein." Pet. 45. According to Petitioner and Dr. Baker, a person of ordinary skill in the art "would have understood that a virtually erased state is an invalid state." *Id.* (citing Ex. 1004 ¶ 223). Patent Owner responds that, "[l]ike claim[] 16, . . . Suda does not disclose invalidation and in fact suggests the opposite" because it discloses in Figures 8 and 9 checking to see whether a physical address associated with an erase command or read request falls within a virtually erased area. PO Resp. 46–48 (citing Ex. 2010 ¶¶ 105–107, 111–113). We disagree with Patent Owner's arguments regarding Figures 8 and 9 for the reasons explained above regarding claim 16. *See supra* Section II.D.3. We note, however, that Petitioner's allegations in the Petition regarding claim 21 mirror those of parent claim 15. *See* Pet. 39–41 (providing the annotated version of Figure 7 of Suda shown above), 45. We agree with Petitioner that storing erasure area pointers in response to an erase command constitutes recording that data stored at the physical address corresponding to the logical block address "can be erased" (claim 15) and also constitutes marking a data packet at that physical address "invalid" (claim 21). *See id.* When a read request is submitted for data in Suda, flash memory controlling section 11 outputs "initial-value data as data to be read" for virtually erased data and outputs "applicable data to be read" for non-virtually erased (i.e., valid) data. *See* Ex. 1003, col. 8, ll. 24–41.

Petitioner has proven, by a preponderance of the evidence, that claim 21 would have been obvious based on Suda under 35 U.S.C. § 103(a).

7. Claim 26

Claim 26 depends from claim 15 and recites three limitations: (1) "the non-volatile storage medium comprises a flash storage medium"; (2) the recited apparatus further comprises "a storage recovery module configured to recover the physical storage location at the physical address"; and (3) the recited apparatus further comprises "a storage module configured to store data associated with another logical identifier on the physical storage location in response to recovering the physical storage location." Petitioner argues that (1) flash memory 14 in Suda is a "flash storage medium"; (2) Suda teaches "eras[ing] the contents of blocks in a storage recovery process whenever the erasure area pointers indicate an entire block contains virtually erased data," citing various examples described in reference to Figures 4, 6, and 8, and a person of ordinary skill in the art would have understood that Suda's system is configured to perform such functions using a "hardware circuit and/or programmable hardware and/or software" (i.e., a "module"); and (3) Suda teaches that after a block is recovered, it "will be mapped with a new logical identifier and then used to store data associated with the new logical identifier" when a write command is received, and a person of ordinary skill in the art would have understood that Suda's system is configured to perform such functions using a "hardware circuit and/or programmable hardware and/or software" (i.e., a "module"). Pet. 45–47.

Patent Owner argues that Suda does not teach or suggest the second limitation because "erasing" is "not the same" as "recover[ing] the physical storage location at the physical address" as recited in the claim. PO Resp. 48 (citing Ex. 2010 ¶ 115); Sur-Reply 20. Patent Owner and Dr. Madisetti, however, do not explain in any detail why that is the case. *See id.* As Petitioner points out, Suda discloses that a virtually erased block can be "set

in an unused state," and "initial-value data" is written to "unused" physical blocks.[11] Ex. 1003, col. 3, ll. 56–63, col. 5, l. 65–col. 6, l. 3; *see* Pet. 46. An "unused" physical block "can be used" again by storing an entry in logical and physical address table 13a indicating a relation between the physical block address and a logical block address. Ex. 1003, col. 3, ll. 41–67 ("[A] physical block the physical block address of which is not related to a logical block address is an unused physical block. In the unused physical block, initial-value data is written. . . . The unused physical block can be used when its physical block address is related to a logical block address in accordance with the control of the flash memory controlling section 11."). Given these disclosures, we credit the testimony of Dr. Baker that a person of ordinary skill in the art would have understood that Suda's "process of returning the physical memory to the point where it can be written again," a form of "garbage collection," constitutes "recover[ing] the physical storage location at the physical address." *See* Ex. 1004 ¶ 240. The physical storage is "recover[ed]" because it is in a state in which it can be written to again. *See* Pet. 46; Reply 17.

Petitioner has proven, by a preponderance of the evidence, that claim 26 would have been obvious based on Suda under 35 U.S.C. § 103(a).

[11] Petitioner also refers to Patent Owner's infringement contentions in responding to Patent Owner's arguments. Reply 17 (citing Ex. 1013). For the reasons explained above, we give no weight to the infringement contentions when determining whether Suda teaches the limitations of the claim. *See supra* Section II.D.2.b.

8. Claims 27–30

Independent claim 27 recites "a request receiver module configured to receive an indication comprising a logical identifier that *is empty*," and independent claim 30 similarly recites "a request receiver module configured to receive an indication that a specified logical identifier *is empty*" and "a read request response module configured to return an indication that the logical identifier *is empty*" (emphasis added). Claims 28 and 29 depend from claim 27. Petitioner in its asserted ground applies Patent Owner's proposed construction from the district court case that the adjective "empty" refers to data identified by the logical identifier, not the logical identifier itself, arguing that Suda's erase command "indicates" that the identified data does not need to be preserved. Pet. 51. We disagree with that interpretation for the reasons explained above. *See supra* Section II.B; Ex. 2006, 2 (concluding that the "logical identifier [that/in the index] is empty" claim language is indefinite). Petitioner does not address claims 27–30 in its Reply.

We cannot ascertain the scope of claims 27 and 30 with reasonable certainty for purposes of assessing patentability and thus cannot reach a decision on the merits with respect to whether Petitioner has established the unpatentability of claims 27–30 over Suda under 35 U.S.C. § 103(a). *See Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, 948 F.3d 1342, 1353 (Fed. Cir. 2020) ("[T]he proper course for the Board to follow, if it cannot ascertain the scope of a claim with reasonable certainty for purposes of assessing patentability, is to decline to institute the [*inter partes* review] or, if the indefiniteness issue affects only certain claims, to conclude that it could not reach a decision on the merits with respect to whether petitioner had established the unpatentability of those claims under sections 102 or

103."); *Marvell Semiconductor, Inc. v. Uniloc 2017 LLC*, IPR2019-01349, Paper 24 at 60 (PTAB Feb. 1, 2021) (final written decision reaching the same conclusion as to certain claims for which the Board could not ascertain their scope with reasonable certainty); *Cisco Sys., Inc. v. Bushnell Hawthorne, LLC*, IPR2019-00750, Paper 13 at 9–10 (PTAB Sept. 24, 2019) (citing prior cases where the scope of the challenged claims could not be determined and the petitioner "had not shown adequately how the prior art applied to the claims," and denying institution based on a district court decision that all of the challenged claims were indefinite).

E. Obviousness Ground Based on Suda and SwSTE'05 (Claims 21, 26, and 28)

1. SwSTE'05

SwSTE'05 is an IEEE journal article entitled "Mapping Structures for Flash Memories: Techniques and Open Problems." Ex. 1010, 1. SwSTE'05 states that "sophisticated data structures and algorithms are required to effectively use flash memories" and provides a survey of "the data structures and algorithms that have been developed for management of flash storage." *Id.*

One technique involves block mapping for improved wear-leveling, where "the block number presented by the host, called a *virtual block number*," is mapped "to a physical flash address called a *sector*." *Id.* at 2. "When a virtual block needs rewritten, the new data does not overwrite the sector where the block is currently stored. Instead, the new data is written to another sector and the virtual-block-to-sector map is updated." *Id.* "[T]here are two kinds of data structures that represent such mappings. . . . [D]irect maps allow efficient mapping of blocks to sectors, and inverse maps allow

efficient mapping of sectors to blocks." *Id.* at 3. "Direct maps are stored at least partially in RAM" and "[i]nverse maps are stored on the flash device itself." *Id.* "When a block is written to a sector, the identity of the block" is also stored "in a header immediately preceding the data" along with other data. *Id.* at 2–3. Figure 1 of SwSTE'05 is reproduced below.

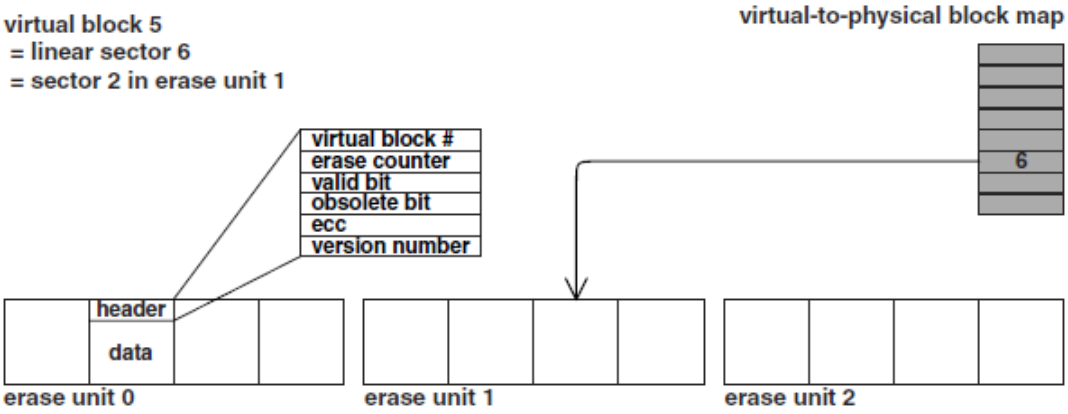

Figure 1 depicts data structures for block mapping in a flash device. *Id.* at 4. SwSTE'05 discloses:

> The gray array on the right [of Figure 1] is the virtual block to physical sector direct map, residing in RAM. Each physical sector contains a header and data. The header contains the index of the virtual block stored in the sector, an erase counter, valid and obsolete bits, and perhaps an error-correction code and a version number. The virtual block numbers in the headers of populated sectors constitute the inverse map, from which a direct map can be constructed.

Id. The valid bit indicates whether a block has been written, such that "the sector is ready for reading." *Id.* at 2.

SwSTE'05 also discloses a reclamation process, stating:

> Over time, the flash device accumulates obsolete sectors and the number of free sectors decrease. To make space for new blocks and for updated blocks, obsolete sectors must be reclaimed. Since the only way to reclaim a sector is to erase an entire unit, reclamation (sometimes called *garbage collection*) operates on entire erase units.

Id. at 5. "Reclamation can take place either in the background (when the CPU is idle) or on-demand when the amount of free space drops below a predetermined threshold." *Id.* The reclamation process involves the following steps:

> One or more erase units are selected for reclamation.
>
> The valid sectors of these units are copied to newly allocated free space elsewhere in the device. Copying the valid data prior to erasing the reclaimed units ensures persistence even if a fault occurs during reclamation.
>
> The data structures that map logical blocks to sectors are updated if necessary, to reflect the relocation.
>
> Finally, the reclaimed erase units are erased and their sectors are added to the free-sector reserve. This stage might also include writing an erase-unit header on each newly-erased unit.

Id.

2. Claim 21

Claim 21 recites that "the marking module is configured to mark a data packet at the physical address invalid." Petitioner argues that the subject matter of claim 21 would have been obvious over the combination of Suda and SwSTE'05,[12] relying on Suda for the limitations of parent claim 15 and SwSTE'05 for the additional limitation of claim 21. Pet. 57–59. Specifically, Petitioner argues that "[t]o the extent that [Patent Owner] argues that Suda's erasure area pointers do not mark data invalid," doing so would have been obvious based on Suda and SwSTE'05, citing SwSTE'05's

[12] Petitioner provides evidence supporting its contention that SwSTE'05 is a prior art printed publication under 35 U.S.C. § 102(b). *See* Pet. 9 (citing Ex. 1004 ¶¶ 58–59; Ex. 1027, 1–2; Ex. 1030 ¶¶ 46–49, 54; Ex. 1034). Patent Owner does not assert otherwise in its Response, and we agree that SwSTE'05 is prior art for the reasons stated by Petitioner.

disclosure of a "valid bit" associated with each block, which indicates whether "the data packets stored in the block are invalid." *Id.* at 57 (citing Ex. 1010, Fig. 1). Petitioner contends that a person of ordinary skill in the art would have been motivated to include valid bits "in either headers of blocks or the index" in Suda and set them as invalid when "a block is designated for erasure, in addition to or instead of using erasure area pointers." *Id.* at 16–17, 58–59. Petitioner provides the following annotated version of Figure 7 of Suda. *Id.* at 59.

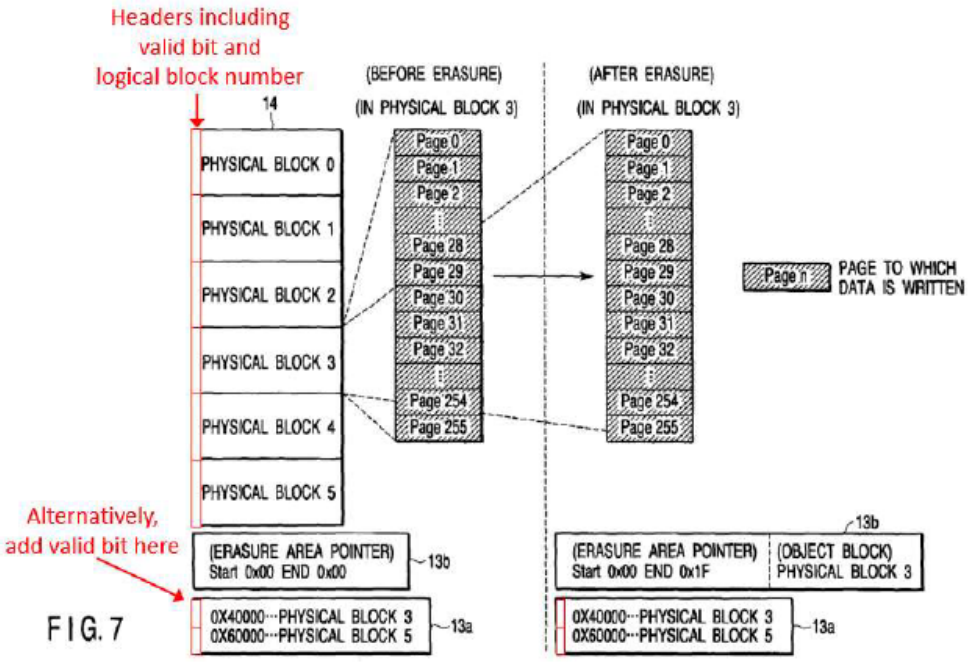

FIG. 7

Annotated Figure 7 depicts where the valid bit would be stored in the asserted combination, i.e., either in the header of each physical block or in the entry for each physical block in logical and physical address table 13a. *Id.* According to Petitioner and Dr. Baker, combining the teachings of Suda and SwSTE'05 in this manner "would have been an obvious modification because both headers and valid bits were standard techniques, and these bits provide useful information for memory systems," and a person of ordinary skill in the art "would have had a reasonable expectation of successfully

using a small fraction of Suda's existing memory, whether RAM and/or flash memory, to store the valid bit associated with each logical block address." *Id.* at 16–17, 58 (citing Ex. 1004 ¶ 235).

Patent Owner makes two arguments. First, Patent Owner contends that a person of ordinary skill in the art would not have been motivated to make the asserted combination, relying on Dr. Madisetti's testimony that

> [v]alid bits are a less desirable approach as it requires marking each individual page rather than simply a range of pages. Given that Suda requires each page to be invalid before it performs the erase, marking each page is inefficient. This is also contrary to the speed goals of Suda.

PO Resp. 50 (quoting Ex. 2010 ¶ 119); Sur-Reply 20–21. We disagree. SwSTE'05 shows that the use of a valid bit to indicate whether a range of flash memory storage is valid or invalid was a well-known technique, and Petitioner has presented persuasive evidence that a person of ordinary skill in the art would have found it advantageous in Suda's system. *See* Pet. 16–17, 58–59; Ex. 1010, 1–4 (presenting a survey of "data structures and algorithms that ha[d] been developed for management of flash storage" by 2005, including the use of a header containing a valid bit with a range of data storage), Fig. 1; Ex. 1004 ¶¶ 234–235. Also, we disagree that adding a single bit in a header for each physical block, or alternatively in each entry in logical and physical address table 13a, as Petitioner proposes, would have been significantly more inefficient than Suda's existing erasure area pointer processes. *See* Ex. 1004 ¶ 235 (testifying that headers including a valid bit and other data provide "valuable information" and only "take up a small amount of existing memory"). "[A]n obviousness showing 'does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the

current invention.'" *Intel Corp. v. Qualcomm Inc.*, – F.4th –, No. 2020-2092, 2022 WL 880681, at *4 (Fed. Cir. Mar. 24, 2022). Petitioner needs to "show only that 'there is something in the prior art as a whole to suggest the *desirability* . . . of making the combination,' not whether there is something in the prior art as a whole to suggest that the combination is the *most desirable* combination available." *Id.*; *see also Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) ("[It is] not necessary to show that a combination is 'the *best* option, only that it be a *suitable* option.'"). Patent Owner's argument that using valid bits was a "less desirable approach" than other approaches of the time, therefore, is unavailing. *See* PO Resp. 50.

Second, Patent Owner argues that Suda and SwSTE'05 do not teach a marking module "configured to mark a data packet at the physical address invalid," as recited in claim 21. PO Resp. 50–51 (citing Ex. 2010 ¶¶ 120, 122); Sur-Reply 21–22. Patent Owner contends that Petitioner's annotated version of Figure 7 (shown above) "does not explain what exactly the valid bits are, where, if any, there are headers in blocks to place the valid bits, how the erasure area pointer would be utilized (if at all), or how the valid bits would specifically 'mark a data packet at the physical address invalid' in Suda." PO Resp. 51. We disagree. SwSTE'05 explains in detail how a "physical sector" (i.e., physical location or physical address) stores data along with a "header" at the beginning of the physical sector that contains, among other things, a "virtual block number" (i.e., logical address) and "valid bit" indicating whether the data of the physical sector is "valid" or "invalid." Ex. 1010, 2–4, Fig. 1. Petitioner explains, with reference to annotated Figure 7, that in the asserted combination, a valid bit as taught by SwSTE'05 would be added in a header to each physical block or each entry

in logical and physical address table 13a. Pet. 57–59. We agree with Petitioner that, given the level of ordinary skill in the art set forth above, a person of ordinary skill in the art would have understood SwSTE'05's valid bit to be a single bit stored in memory and would have understood that the device would check that bit to determine whether the associated range of data is "valid" or "invalid." *See id.*; Reply 18–19; Ex. 1004 ¶¶ 234–235; *supra* Section II.A. Thus, we are persuaded that the combination of Suda and SwSTE'05 teaches a marking module "configured to mark a data packet at the physical address invalid."[13]

Patent Owner further argues that Petitioner fails to provide a motivation for a person of ordinary skill in the art to "alter Suda's system to include valid bits." PO Resp. 51 (quoting Ex. 2010 ¶ 122). As explained above, however, Petitioner has provided a sufficient motivation to combine Suda and SwSTE'05, supported by the testimony of Dr. Baker, which we credit.

Petitioner has proven, by a preponderance of the evidence, that claim 21 would have been obvious based on Suda and SwSTE'05 under 35 U.S.C. § 103(a).

3. Claim 26

Claim 26 depends from claim 15 and recites three limitations: (1) "the non-volatile storage medium comprises a flash storage medium"; (2) the recited apparatus further comprises "a storage recovery module configured to recover the physical storage location at the physical address";

[13] We also are persuaded that Suda alone teaches the limitation of claim 21. *See supra* Section II.D.6.

and (3) the recited apparatus further comprises "a storage module configured to store data associated with another logical identifier on the physical storage location in response to recovering the physical storage location." Petitioner argues that the subject matter of claim 26 would have been obvious over the combination of Suda and SwSTE'05, relying on Suda for the limitations of parent claim 15 and the first and third limitations of claim 26, and SwSTE'05 for the second limitation of claim 26. Pet. 59–61.

With respect to the second limitation, Petitioner argues that "Suda's system operates as a 'garbage collection' process to reclaim erase units (Suda's blocks)." *Id.* at 60. Alternatively, Petitioner points to the four-step process described in SwSTE'05 for erase unit reclamation, and argues that the "last step of physically erasing the erase unit will 'recover the physical storage location,' as claimed." *Id.* According to Petitioner and Dr. Baker, a person of ordinary skill in the art would have been motivated to apply SwSTE'05's process to Suda, "recognizing that the 'erase units' of SwSTE'05 are Suda's 'blocks,' and that the 'data structures that map logical blocks to sectors' of SwSTE'05 are Suda's tables 13a and 13b," and "would have had a reasonable expectation of success because garbage collection was well-known and had been a standard part of flash memory management since the mid-1990s."[14] *Id.* at 16–17, 60–61 (quoting Ex. 1010, 5; citing Ex. 1004 ¶ 241).

[14] Petitioner also refers to Patent Owner's infringement contentions in arguing that the second limitation of claim 26 is taught by Suda and SwSTE'05. Pet. 59 (citing Ex. 1013). For the reasons explained above, we give no weight to the infringement contentions when determining whether the references teach the limitations of the claim. *See supra* Section II.D.2.b.

Patent Owner argues that by referring to "garbage collection," Petitioner fails to account for the claim language of the second limitation and does not "describe how Suda or SwSTE'05 would disclose this limitation." PO Resp. 52. Petitioner, however, asserts that a person of ordinary skill in the art would have been motivated to use SwSTE'05's reclamation process in Suda, and specifically identifies the last step of that process as "recover[ing] the physical storage location at the physical address." *See* Pet. 60. Suda describes the last step as follows: "Finally, the reclaimed erase units are erased and their sectors are added to the free-sector reserve." Ex. 1010, 5.

Patent Owner also contends that a person of ordinary skill in the art would not have been motivated to make the asserted combination, relying on Dr. Madisetti's testimony that Petitioner "fails to identify any reason why a [person of ordinary skill in the art] would be motivated to include the garbage collection process from SwSTE'05 in Suda especially given the fact that Petitioner alleges Suda already had a garbage collection process." PO Resp. 52–53 (quoting Ex. 2010 ¶ 124); Sur-Reply 22–23. We disagree. Petitioner makes alternative arguments—namely, that (1) Suda's erasing of a block when the erasure area pointers indicate that the entire block contains virtually erased data constitutes "recover[ing] the physical storage location at the physical address,"[15] but if not, (2) SwSTE'05 teaches the well-known, standard process of garbage collection that a person of ordinary skill in the art would have been motivated to use to "free up space in memory so that it can be used again." *See* Pet. 16–17, 60–61; Ex. 1004 ¶¶ 240–242. We agree

[15] As explained above, we are persuaded that Suda alone teaches the second limitation of claim 26. *See supra* Section II.D.7.

that garbage collection was a well-known technique and would have operated in and improved Suda's system in the same way it does in SwSTE'05, allowing storage to be "reclaimed" and added to the reserve of available storage for writing to in the future. *See id.*; Ex. 1010, 5; *supra* Section II.A (the parties' agreed definition of the level of ordinary skill in the art includes knowledge of "how garbage collection is used with flash memory"). We again credit Dr. Baker's testimony on that point, as it is consistent with the cited references and the level of ordinary skill in the art, and supported by other evidence in the record. *See* Ex. 1004 ¶¶ 74–76 (citing Exs. 1009–11, 1020), 240–242; *supra* Section II.A. Dr. Baker explains, for example, that "[g]arbage collection greatly improves the on-demand operational speed of flash memory devices" because "garbage collection can conduct the relatively slower erasures during a background process. That erased memory can then be written to on-demand at relatively fast speeds. Without garbage collection, an area of memory might first need to be erased before writing, taking orders of magnitude longer." Ex. 1004 ¶ 75. Those same advantages would apply if SwSTE'05's process were incorporated into Suda (to the extent Suda does not already perform garbage collection).

Petitioner has proven, by a preponderance of the evidence, that claim 26 would have been obvious based on Suda and SwSTE'05 under 35 U.S.C. § 103(a).

4. Claim 28

Claim 28 depends from claim 27. We cannot ascertain the scope of claim 28 with reasonable certainty for purposes of assessing patentability due to the "empty" phrase in parent claim 27 and thus cannot reach a

decision on the merits as to Petitioner's asserted ground based on Suda and SwSTE'05. *See supra* Section II.D.8.

F. Obviousness Ground Based on Bennett (Claims 15–21 and 26–30)

Petitioner contends that claims 15–21 and 26–30 are unpatentable over Bennett under 35 U.S.C. § 103(a). Pet. 17–36. In the Decision on Institution, we determined based on the record at the time that Petitioner had not established a reasonable likelihood of prevailing on its asserted ground as to claims 15–21 and 26, and we could not ascertain the scope of claims 27–30 with reasonable certainty for purposes of assessing patentability due to the "empty" phrases in independent claims 27 and 30, such that a meaningful review of Petitioner's asserted ground could not be performed. Dec. on Inst. 28–35. As explained above, we conclude that claims 15–21 and 26 are unpatentable under the Suda-based grounds. *See supra* Sections II.D–E. As such, we need not address Petitioner's alternative ground based on Bennett. *See Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. Apr. 30, 2020) (non-precedential) (recognizing that "the Board need not address issues that are not necessary to the resolution of the proceeding" and, thus, agreeing that the Board has "discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims"). With respect to claims 27–30, we cannot ascertain the scope of the claims with reasonable certainty and thus cannot reach a decision on the merits as to Petitioner's asserted ground based on Bennett. *See supra* Sections II.D.8, II.E.4.

III. CONCLUSION[16]

Petitioner has demonstrated, by a preponderance of the evidence, that claims 15–21 and 26 of the '406 patent are unpatentable. We cannot ascertain the scope of claims 27–30 with reasonable certainty for purposes of assessing patentability and thus cannot reach a decision on the merits with respect to whether Petitioner has established unpatentability of those claims under 35 U.S.C. § 103(a).

[16] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. §§ 42.8(a)(3), 42.8(b)(2).

In summary:

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
15–21, 26–30	103(a)	Suda	15–21, 26	
21, 26, 28	103(a)	Suda, SwSTE'05	21, 26	
15–21, 26–30	103(a)	Bennett[17]		
Overall Outcome			15–21, 26[18]	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 15–21 and 26 of the '406 patent have been shown to be unpatentable.

This is a final decision. Parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

[17] As explained above, given our disposition of the grounds based on Suda and the combination of Suda and SwSTE'05, we do not reach Petitioner's alternative ground asserting that claims 15–21 and 26 are unpatentable over Bennett. *See supra* Section II.F.

[18] As explained above, we cannot ascertain the scope of claims 27–30 with reasonable certainty for purposes of assessing patentability and thus cannot reach a decision on the merits with respect to whether Petitioner has established unpatentability of claims 27–30 under 35 U.S.C. § 103(a). *See supra* Sections II.D.8, II.E.4, II.F.

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