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Paper No. 10
Date: February 15, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VOLKSWAGEN GROUP OF AMERICA, INC.,
Petitioner,

v.

ARIGNA TECHNOLOGY LTD.,
Patent Owner.

IPR2021-01321
Patent 8,247,867 B2

Before GARTH D. BAER, SHARON FENICK, and IFTIKHAR AHMED, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Volkswagen Group of America, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet."), requesting an *inter partes* review of claims 1–9 (the "challenged claims") of U.S. Patent No. 8,247,867 B2 (Ex. 1001, "the '867 Patent"). Arigna Technology Ltd. ("Patent Owner") filed a Preliminary Response to the Petition (Paper 9, "Prelim. Resp.").

We have authority under 35 U.S.C. § 314 to determine whether to institute *inter partes* review. For the reasons discussed below, we institute *inter partes* review.

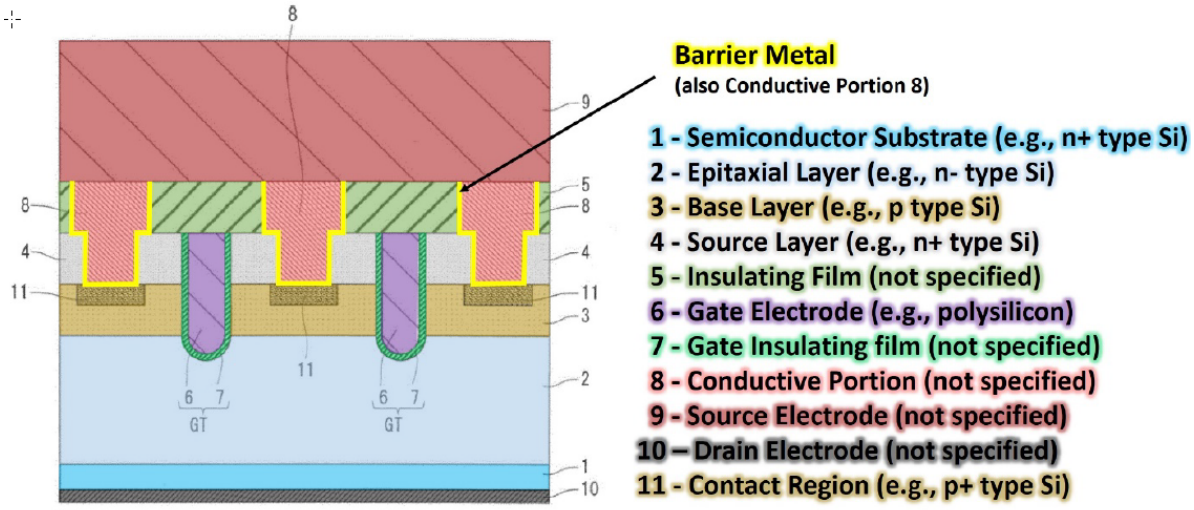
II. BACKGROUND

A. RELATED MATTERS

The '867 patent is at issue in *Arigna Technology Limited v. Volkswagen AG et al.,* Case No. 2:21-cv-00054-JRG-RSP (E.D. Tex.); ITC Proceeding 337-TA-1267 ("ITC proceeding"); and IPR2021-01382.

B. THE '867 PATENT

The '867 patent is directed to a semiconductor device. Ex. 1001, code (54). The '867 patent's Figure 1, with Petitioner's annotations, is reproduced below.



EX1001, Fig. 1 (annotated)

Pet. 31. Figure 1 illustrates a cross-section of a semiconductor device. *Id*. at 3:35–54. The device has an n+-type substrate 1 (*id.* at 4:4–5); n-type drift layer 2 (*id*. at 4:6–10); p-type base 3 (*id*. at 4:13–14); n+-type source 4 (*id.* at 4:14–16); insulating film 5 (*id.* at 4:31–32); gate electrode 6 (*id.* at 4:19–30); gate insulating film 7 (*id.* at 4:19–30); conductive portions 8 (*id.* at 4:32–33); source electrode 9 (*id.* at 4:59–67); drain electrode 10 (*id.* at 4:5–6); and p+-type contact region 11 in base 3 (*id.* at 4:39–46).

C. Challenged Claims

Petitioner challenges claims 1–9. Claims 1, 4, and 8 are independent. Independent claim 1 is representative and is reproduced below:

> 1. A semiconductor device, comprising:
>
> a base layer having a first conductivity type;
>
> a source layer formed on said base layer and having a second conductivity type;
>
> an insulating film formed on said source layer;
>
> a plurality of gate structures penetrating said base layer;

> a plurality of conductive portions penetrating said insulating film and said source layer and electrically connected to said source layer and said base layer; and
>
> a source electrode formed on said insulating film and electrically connected to said conductive portions, wherein:
>
> said gate structures are formed in a stripe shape in plan view;
>
> parts in which said conductive portions are connected to said base layer are formed, in plan view, with a distance from said gate structures between said gate structures so as to be parallel to a direction of said stripe shape of said gate structures; and
>
> a dimension of a part in which said source layer and said base layer are in contact with each other between said gate structures and said conductive portions are 0.36 μm or more and 0.43 μm or less.

Ex. 1001, 12:19–40.

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 54.

Reference(s)	Basis	Challenged Claims
Torii[1]	§ 102	4, 7
Torii, Hebert[2]	§ 103	5
Torii, Hebinuma[3]	§ 103	6
Kim03[4]	§ 102	8, 9

[1] WO 2009/060670 A1, Pub. May 14, 2009 (Translation) (Ex. 1030, "Torii").
[2] US 2009/0218619 A1, Pub. Sep. 3, 2009 (Ex. 1025, "Hebert").
[3] JP 2006-59940, Pub. Mar. 2, 2006 (Translation) (Ex. 1027, "Hebinuma")
[4] J. Kim et al., High-Density Trench MOSFETs Employing Two Step Trench Technique and Trench Contact Structure, Proceedings of the 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs, pp. 165–67 (2003) (Ex. 1034, "Kim03").

Sekiguchi,[5] Hebert	§ 103	8, 9
Kim03, Sekiguchi	§ 103	1–3
Sekiguchi, Williams99[6]	§ 103	1, 3
Sekiguchi, Williams99, Hebert	§ 103	2

Petitioner also relies on a declaration from Dr. Sanjay K. Banerjee (Ex. 1002).

III. DISCRETIONARY DENIAL UNDER 35 U.S.C. § 314(a)

A. DENIAL BASED ON EXCESSIVE GROUNDS

Patent Owner asserts we should exercise our discretion to deny this Petition "due to the disproportionately voluminous filings and lack of particularity in the Petition." Prelim. Resp. 68. Specifically, Patent Owner asserts that the Petition imposes an undue burden on Patent Owner and the Board because "[t]he number of asserted grounds and references is disproportionately large when compared with the number of distinct challenged claims." *Id*. at 69 (quoting *Adaptics Ltd. v. Perfect Co.*, IPR2018-01596, Paper 20 at 20–22 (P.T.A.B. March 6, 2019) (informative)). Patent Owner further objects to Petitioner's "voluminous filings" including Petitioner's 117-page Petition, 439-page declaration, and 69 exhibits to challenge a total of just nine claims. *Id*. at 68. Last, Patent Owner asserts "**each** of the independent claim grounds suffers from a lack of particularity." *Id*. at 69.

We disagree. As to Petitioner's allegedly "voluminous filings," the Petition's 13,512 words is within the Board's 14,000 word-count limit. *See*

[5] US 2009/0179261 A1, Pub. Jul. 16, 2009 (Ex. 1044, "Sekiguchi").
[6] US 6,413,822 B2, Jul. 2, 2002 (Ex. 1033, "Williams99").

37 C.F.R. § 42.24(a)(1)(i). In addition, we do not fault Petitioner for its long expert declaration or for the large number of supporting exhibits. Because the challenged patent's subject matter is complex, Petitioner's challenge requires extensive explanation. *See, e.g.*, Pet. 1–30 (providing thirty pages of technology background). Moreover, the declaration's length and supporting exhibits may have burdened Petitioner, but they do not, on their own, impose any undue burden on the Board or on Patent Owner. Next, we find Petitioner's number of grounds—no more than two distinct challenges for each challenged claim—does not overly burden the Board. Last, we disagree with Patent Owner that Petitioner's grounds suffer from a lack of particularity for the reasons explained below in Sections IV.D.1 and IV.D.4.a. We therefore decline to exercise our discretion to deny institution.

B. DENIAL BASED ON *FINTIV*

Patent Owner contends the Board should deny the Petition under § 314(a) "[g]iven the advanced state of the [parallel] ITC Proceeding—which addresses the same issues raised in the instant Petition." Prelim. Resp. 71. For the reasons that follow, we decline to exercise our discretion to deny the Petition on that basis.

The Board's precedential decision in *Apple Inc. v. Fintiv Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"), identifies a non-exclusive list of factors parties may consider addressing where there is a related, parallel district court action to determine whether such action provides any basis for discretionary denial. *Fintiv*, Paper 11 at 5–16. Those factors include:

> 1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;

> 2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
>
> 3. investment in the parallel proceeding by the court and the parties;
>
> 4. overlap between issues raised in the petition and in the parallel proceeding;
>
> 5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
>
> 6. other circumstances that impact the Board's exercise of discretion, including the merits.

Id. at 5–6.

In evaluating the factors, we take a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review. *Id.* at 6.

1. Factor 1

Neither party has sought a stay in the ITC proceeding, and we do not speculate about the likelihood of one. This factor is neutral.

2. Factor 2

The ITC proceeding has a November 28, 2022 target date for completion, which is approximately three months before the deadline for a final written decision in this proceeding. Ex. 2004, 4. Petitioner notes that "the ITC presently has only three ALJs following ALJ Lord's retirement," and "the ITC investigation may be reassigned and/or rescheduled when the ITC welcomes a fourth ALJ." Pet. 114. In response, Patent Owner asserts that the investigation has already been reassigned to a newly hired ALJ who has issued an updated scheduling order that maintains the November 28 targeted completion date. Prelim. Resp. 74. In these circumstances, we decline to speculate on further delay for the ITC proceeding. Even so, given

the proximity between the projected ITC proceeding's completion date and the final written decision due date, on balance this factor at most weighs only slightly in favor of exercising our discretion to deny the Petition.

3. Factor 3

Patent Owner argues that there has been significant investment in the ITC Proceeding because "[t]he parties have already filed their *Markman* briefs and notices of prior art," and by the time this institution decision issues, "fact and expert discovery will be complete, and the summary judgment deadline will have passed." Prelim. Resp. 75. On the other side, Petitioner notes—and Patent Owner does not contest—that Petitioner "filed this Petition . . . almost immediately following institution of the ITC investigation." Pet. 115; *see* Prelim. Resp. 75. In these circumstances, we find this factor neutral.

4. Factor 4

As Petitioner notes, the issues in this case are somewhat different than the parallel ITC proceeding because only four of the nine challenged claims in this Petition are also at issue in the ITC proceeding. *See* Pet. 115. Moreover, as Petitioner further notes, "the ITC lacks the authority to invalidate the '867 Patent." *Id*. We agree with Petitioner that the additional claims at issue here, but not in the ITC proceeding, weigh against exercising our discretion to deny institution. Thus, we determine this factor weighs against denying institution.

5. Factor 5

Neither party disputes that Petitioner and Patent Owner are parties to the ITC proceeding. Thus, this factor favors exercising our discretion to deny institution.

6. Factor 6

Petitioner asserts "[t]he merits are exceptionally strong, and the ITC lacks the authority to invalidate the '867 Patent." Pet. 115. Patent Owner contends "the merits of this Petition are particularly weak." Prelim. Resp. 76. As outlined below, we largely agree with Petitioner's analysis. However, there are a number of factual disputes to be resolved at trial. Thus, while we determine that the merits meet the standard for institution of *inter partes* review, we do not agree with either party that they are either particularly strong or weak. Thus, we find that this factor is neutral.

7. Summary and Conclusion

We have considered the circumstances and facts before us in view of the *Fintiv* factors. For the reasons given, we are not persuaded to exercise our discretion to deny institution.

IV. ANALYSIS

A. LEVEL OF SKILL IN THE ART

Petitioner contends a person of ordinary skill in the art "would have possessed (1) the equivalent of a Master of Science degree in electrical engineering, materials science, physics, or equivalent; (2) working knowledge of power semiconductors and semiconductor processing; and (3) at least two years of experience in related semiconductor processing, analysis, design, or development." Pet. 54–55. Further, "[a]dditional education could substitute for professional experience, and significant work experience could substitute for formal education." *Id*. at 55. At this stage, Patent Owner does not provide a description of the person of ordinary skill.

Petitioner's description is consistent with the prior art and patent specification before us and is supported by credible expert testimony. *See*

Okajima v. Bourdeau, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). For the purpose of our decision, we adopt Petitioner's description.

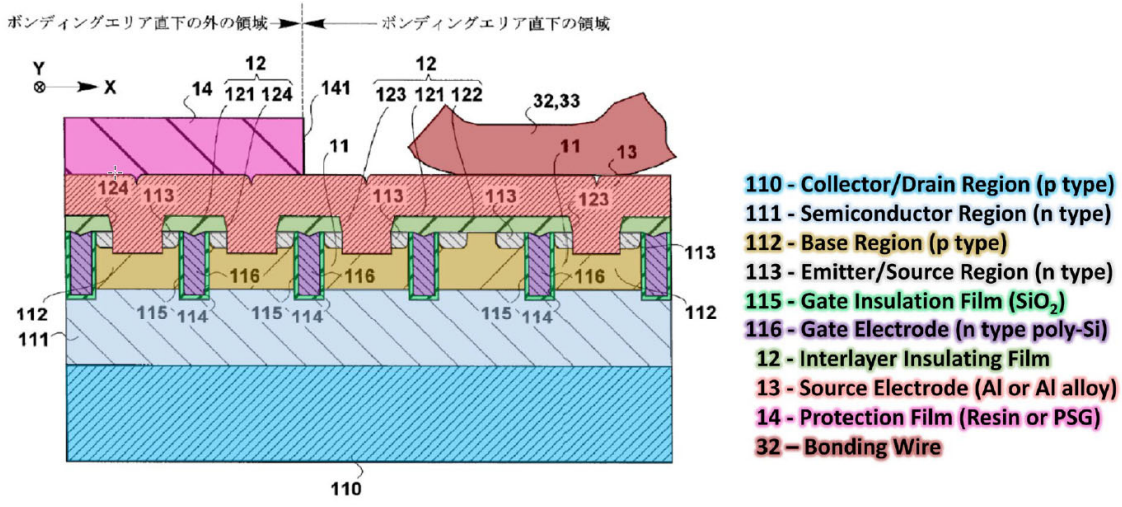
B. Claim Construction

Neither party proposes any claim terms for construction. Pet. 55; Prelim. Resp. 20. We determine we need not explicitly construe any terms to determine whether to institute an *inter partes* review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Description of Principal Prior Art References

1. Torii (Ex. 1030)

Torii discloses a semiconductor device. Ex. 1030, code (54). Torii's Figure 11, with Petitioner's annotations, is reproduced below.



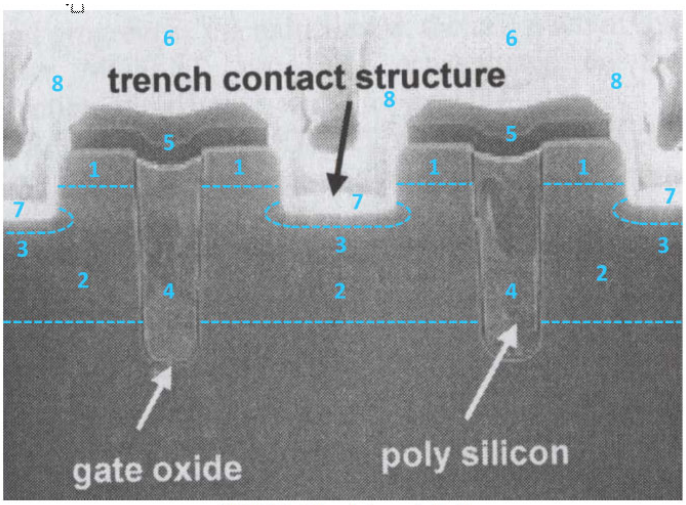
[upper-left] REGION OUTSIDE OF DIRECTLY BELOW BONDING AREA
[upper-right] REGION DIRECTLY BELOW BONDING AREA

EX1030, Fig. 11 (annotated)

Pet. 41. Figure 11 is a semiconductor device with the elements noted above. Ex. 1030 ¶ 78; *see* Ex. 1002 ¶ 197 (citing Ex. 1030 ¶¶ 38–43, 55–56, 80, 90, 92, 93, Fig. 11).

2. Kim03 (Ex. 1034)

Kim03 teaches a Depletion Trench Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Ex. 1034, 4.[7] Kim03's Figure 5, with Petitioner's annotations, is reproduced below.



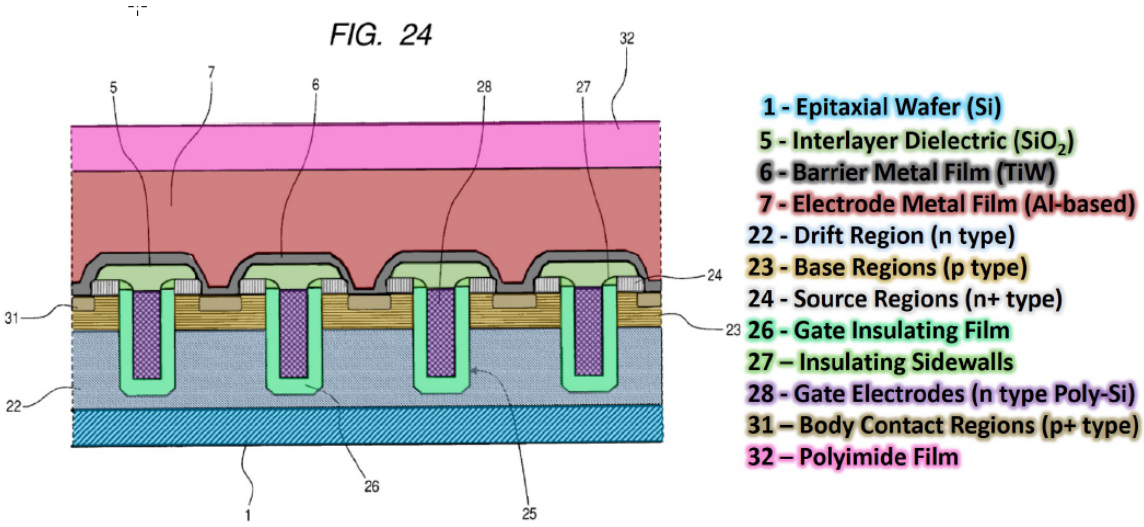
EX1034, Fig. 5 (annotated)

Pet. 44. Figure 5 is a trench Depletion MOSFET or DMOSFET device. Ex. 1034, 6. It includes (1) n+-type source regions; (2) p-type body regions with (3) a p+-type contact landing; (4) a trenched gate; (5) interlayer insulator; and (6) source/body metallization with (7) a barrier metal and (8) at least one additional metal layer. Ex. 1002 ¶¶ 111–125, 186.

3. Sekiguchi (Ex. 1044)

Sekiguchi teaches a semiconductor device. Ex. 1044, code (54). Sekiguchi's Figure 24, with Petitioner's annotations, is reproduced below.

[7] We cite to Petitioner's provided page numbering.



EX1044, Fig. 24 (annotated)

Pet. 48. Figure 24 is a semiconductor with the elements noted above. Ex. 1044 ¶ 41; *see* Ex. 1002 ¶ 195 (citing Ex. 1044, 98–105).

D. OBVIOUSNESS ANALYSIS

1. Anticipation of Claims 4 and 7 based on Torii

Petitioner contends Torii anticipates claims 4 and 7. Pet. 59–66. Based on Petitioner's analysis and for the reasons explained below, we find Petitioner has, at this stage, demonstrated a reasonable likelihood of prevailing on this challenge. Patent Owner raises several arguments contesting Petitioner's challenge. We discuss those arguments below.

a. Torii's Different Embodiments

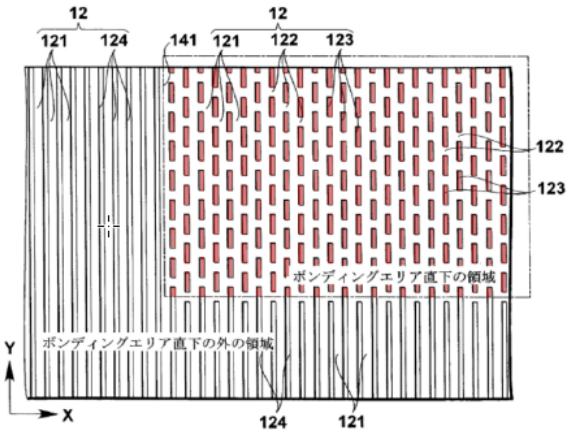
Patent Owner asserts that Petitioner's anticipation challenge fails because Petitioner improperly "mixes and matches features from different Torii embodiments." Prelim. Resp. 22. Specifically, according to Patent Owner, in mapping Torii's disclosures to claim 4, Petitioner relies on Torii's figures 3, 5, and 9–11, even though figures 3 and 5 are separate (and incompatible) embodiments not only from each other, but also from Torii's

embodiment shown in figures 9–11 ("Fig. 9–11 embodiment"). Prelim. Resp. 22–28.

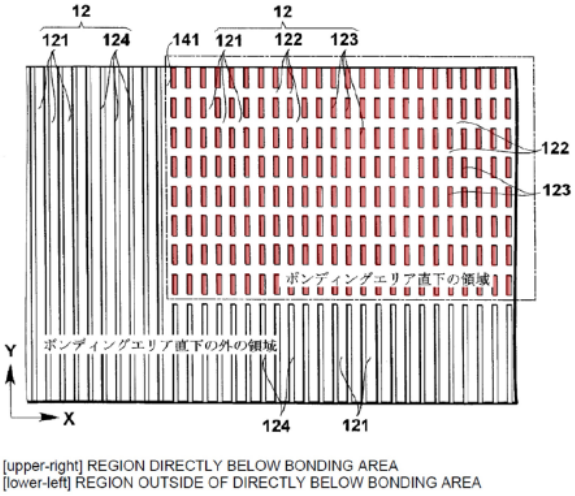
We disagree with Patent Owner's argument. First, in mapping Torii's disclosures to claim 4, Petitioner relies on Torii's Fig. 9–11 embodiment. *See* Pet. 59–66. For one limitation, Element [4.8] ("conductive portions . . . are formed, in plan view, side by side in an island shape in a direction of said stripe"), Petitioner cites Torii's Fig. 9–11 embodiment as well as Figs. 3 and 5 to show Torii teaches the claimed side-by-side island-shaped conductive portions. *Id*. at 64. Because, as outlined in the section immediately below, on this record we agree with Petitioner that Torii's Fig. 9–11 embodiment teaches the claimed side-by-side, island-shaped conductive portions (i.e. claim Element [4.8]), we do not agree that citing Figs. 3 and 5 as *additional* support is fatal to Petitioner's challenge.

b. Claim Element [4.8]

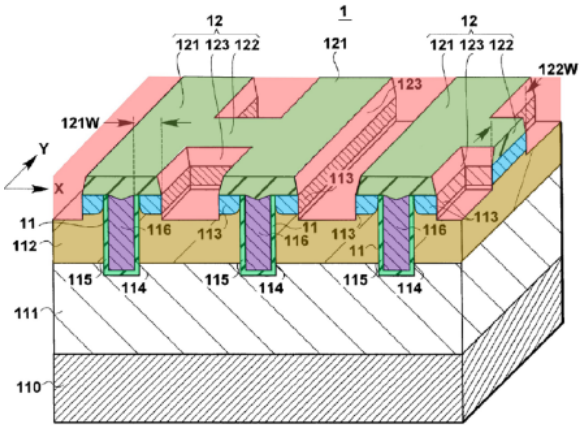
Element [4.8] recites "parts in which said conductive portions are connected to said base layer are formed, in plan view, side by side in an island shape in a direction of said stripe shape of said gate structures with a distance from said gate structures between said gate structures." Ex. 1001, 12:65–13:2. Petitioner asserts that Torii's Figures 3, 5, 9 and 10 (reproduced below with Petitioner's added coloring) teach this side-by-side conductive-portions feature because "[aperture parts 123] repeat along the direction of the striped gates, as shown in pink below." Pet. 64.



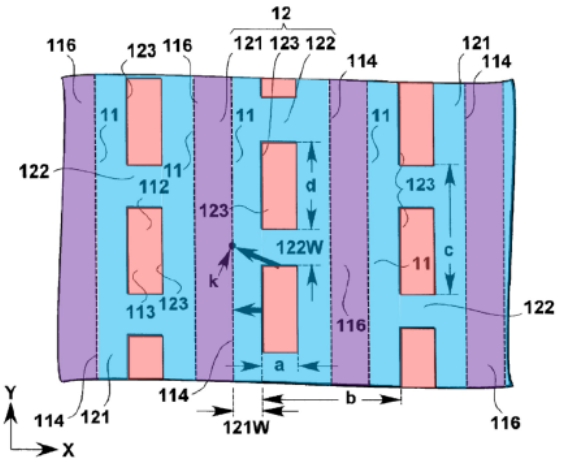
EX1030, Fig. 3 (annotated)



EX1030, Fig. 5 (annotated)



EX1030, Fig. 9 (annotated)



EX1030, Fig. 10 (annotated)

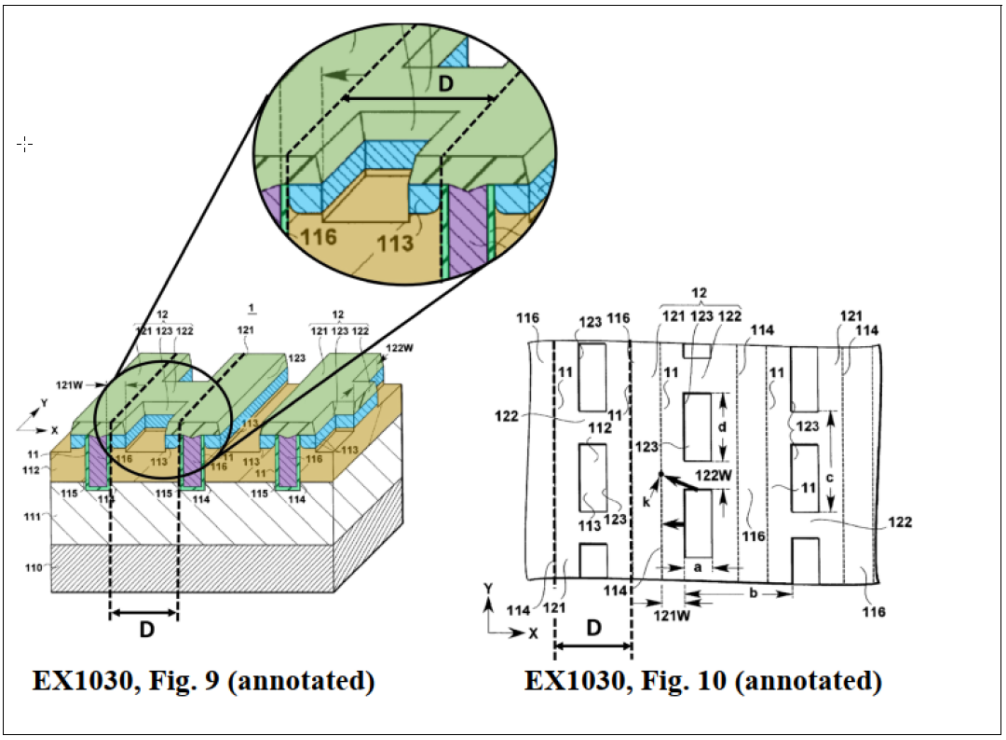
Patent Owner argues that Petitioner's challenge fails because the Petition is unclear as to whether the side-by-side limitation requires a straight-line configuration (as in Torii's Fig. 5) or whether an offset configuration (as depicted in Torii's Figs. 3 and 9) would suffice.

We disagree with Patent Owner's argument. Because the Petition references both the straight-line configuration and the offset configuration, we find the Petition is sufficiently clear in its assertion that *either* configuration meets the claimed side-by-side limitation. Based on the current record, we agree with Petitioner's assertion—both configurations

depict "conductive portions . . . are formed, in plan view, side by side in an island shape in a direction of said stripe shape of said gate" as claim element 4.8 requires. We note that in its Preliminary Response, Patent Owner never explicitly contests that Torii's offset configuration (as depicted in Figs. 3 and 10) discloses the claimed "side-by-side" feature. *See* Prelim. Resp. 29, 31 (arguing that "Arigna is unable to address Petitioner's theory because Petitioner has failed to describe it with any particularity" and "Arigna cannot be expected to address every possible permutation of what Petitioner might have meant with its vague invalidity grounds"). If Patent Owner chooses to assert this argument, we will address it during the balance of this proceeding.

c. *Claim Element [4.9]*

Element [4.9] requires "a dimension of a part in which said source layer and said base layer are in contact with each other between said gate structures in a region in which said conductive portions are not connected to said base layer is 0.36 μm or more." Ex. 1001, 13:3–7. According to Patent Owner, Petitioner fails to demonstrate that Torii teaches the claimed ≥ 0.36 μm dimension because "Petitioner's explanation for how this limitation is met is limited to a single sentence—'Torii discloses the claimed dimension D (below) can be 1.5μm' and two annotated figures: [reproduced below]."



EX1030, Fig. 9 (annotated)

EX1030, Fig. 10 (annotated)

Prelim. Resp. 31–32 (citations omitted).

We disagree with Patent Owner's argument. As support for its argument that Torii discloses the claimed dimension D can be 1.5µm, Petitioner cites paragraph 345 of Dr. Banerjee's Declaration, as well as relevant disclosures in Torii. Pet. 65 (citing Ex. 1030 ¶¶ 46, 89, Figs. 9, 10; Ex. 1002 ¶ 345). Paragraph 345 of Dr. Banerjee's Declaration explains precisely how Torii teaches the claimed dimension:

> The relevant dimension is the mesa width, labeled "D" in the figures below. *See* Torii at Figs. 9, 10. As Figure 10 below illustrates, the mesa width D is equal to 121W + a + 121W. Torii discloses an example in which dimension "121W" is 0.5 µm and dimension "a" is 0.5 µm. *See* Torii at ¶ [0089]; *see also id.* at ¶ [0046]. With these dimensions, Torii's disclosed mesa width D is 1.5 µm, which is larger than 0.36 µm.

Ex. 1002 ¶ 345.

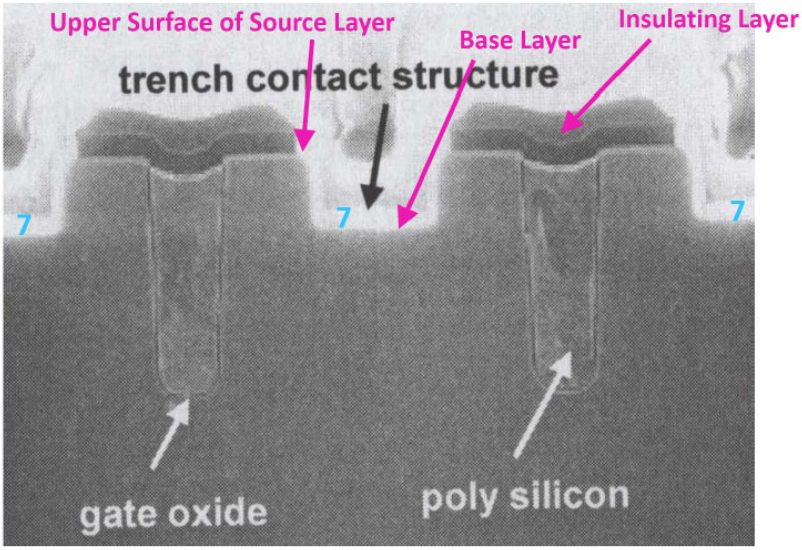
Patent Owner does not contest Dr. Banerjee's assertion. *See* Prelim. Resp. 31–34. Instead Patent Owner asserts (in a footnote) that Petitioner improperly incorporates Dr. Banerjee's argument into the Petition. *See id*. at 34 n.6. We disagree that Petitioner's argument improperly incorporates Dr. Banerjee's argument. While our rules preclude incorporating entire arguments by reference, they do not preclude what Petitioner has done here—i.e., assert in the Petition how and where Torii discloses the claimed feature, while providing additional details related to those calculations in a supporting declaration.

2. Anticipation of Claims 8 and 9 based on Kim03

Petitioner contends Kim03 anticipates claims 8 and 9. Pet. 74–81. Based on Petitioner's analysis and for the reasons explained below, we find Petitioner has, at this stage, demonstrated a reasonable likelihood of prevailing on this challenge.

a. Claim Element [8.5]

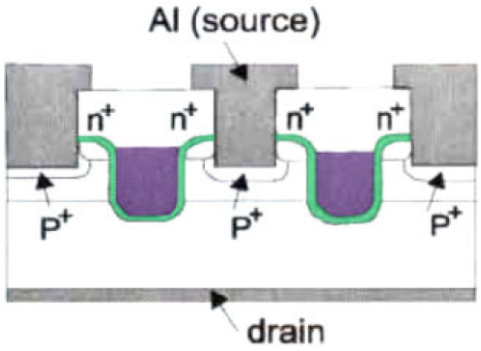
Element [8.5] requires "a conductive portion penetrating said insulating film and said source layer, being in contact with an upper surface of said source layer, and electrically connected to said source layer and said base layer." Ex. 1001, 14:7–10. Petitioner asserts Kim03 includes this feature because Figure 5 (reproduced below with Petitioner's annotations) depicts a thin barrier metal (7) that "penetrates the insulating film and source, contacts a stair-stepped upper surface of the source, and electrically connects to the source and base." Pet. 77.



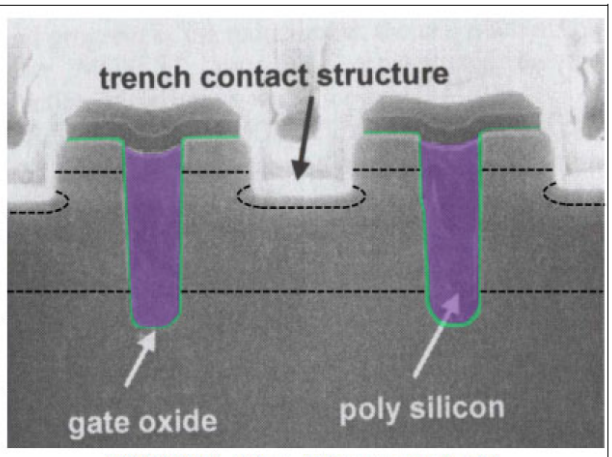
EX1034, Fig. 5 (annotated)

Pet. 78.

Patent Owner asserts that Petitioner's challenge fails because Petitioner's theory is "based solely on an oblique (downward angle) image with no consideration for the parallax error inherent in such images, and no explanation as to the apparent conflict with the other Kim03 figures which clearly show no stair step or upper surface." Prelim. Resp. 39–40. In addition, Patent Owner argues, Kim03 does not teach Element [8.5] because "Kim03 teaches that a gate oxide layer is deposited on the upper surface of the source, which would prevent contact between the purported conductive portion and upper surface of the source," and "Petitioner's own annotated figures [reproduced below] show the gate oxide (green) covering the entire upper surface of the source:"



EX1034, Fig. 1(e) (annotated)



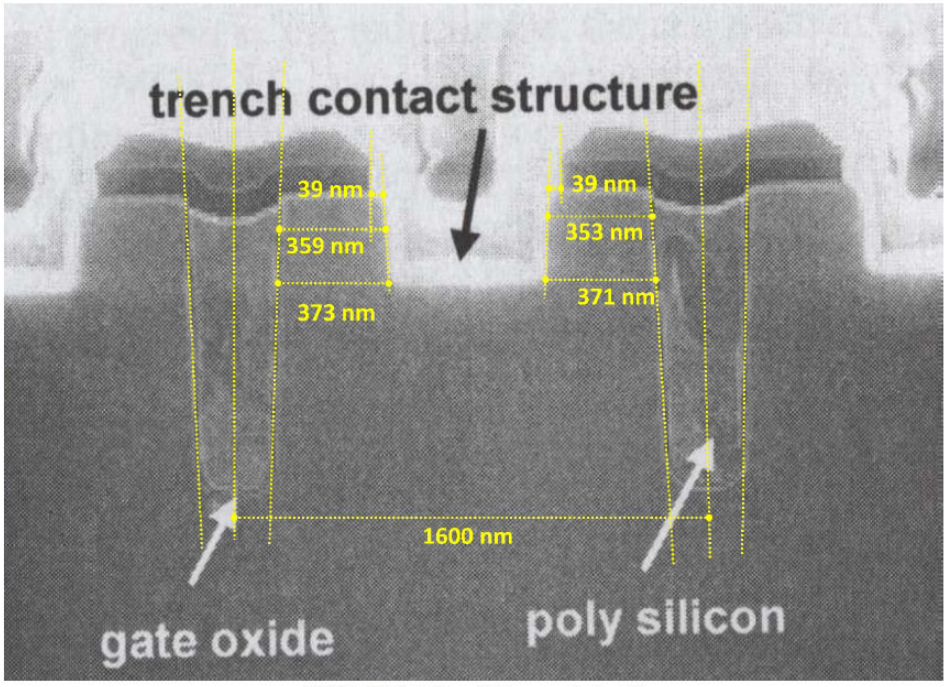
EX1034, Fig. 5 (annotated)

Prelim. Resp. 40–41.

We disagree with Patent Owner's arguments. To the extent that Patent Owner asserts the apparent stair-stepped upper surface of the source in Figure 5 is instead just a parallax error in the image, that is a factual issue better suited for resolution on a full record at trial. Further, we disagree with Patent Owner that the apparent stair-stepped upper surface in Kim03's figure 5 conflicts with the additional figures in Kim03. Rather, it appears the other figures simply lack the detail depicted in figure 5. Nothing in the additional cited figures affirmatively precludes stair-stepped upper surface depicted in Kim03's figure 5, as Patent Owner suggests. As to Patent Owner's argument that the gate oxide (green) covers the entire upper surface of the source and thus prevents contact between the purported conductive portion and upper surface of the source, it does not appear that the gate oxide covers the entire upper surface of the source in Petitioner's annotated Figure 5. To the extent Patent Owner disagrees, the extent of the gate oxide layer is a factual issue best resolved on a full record at trial.

b. Claim Element [8.7]

Element [8.7] requires "a dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other is 10 nm or more and 40 nm or less." Ex. 1001, 14:13–16. Petitioner asserts Kim03's Figure 5 depicts this claimed dimension because Kim03 teaches that the structure in Figure 5 has "unit cells with a cell pitch of 1.6 μm" and "[t]his provides scale for Figure 5." Pet. 80. Using that scale, Petitioner asserts that Figure 5 (reproduced below, Petitioner's annotations)) depicts a 39nm stairstep, which is within the claimed range. *Id.*; *see id.* at 81.



EX1034, Fig. 5 (annotated)

Patent Owner contests whether Kim03 teaches the claimed 10nm–40nm dimension. According to Patent Owner, "in the copy of Kim03 submitted as evidence, the resolution of the image in Figure 5 is so low as to make the kind of calculations purportedly performed by Petitioner

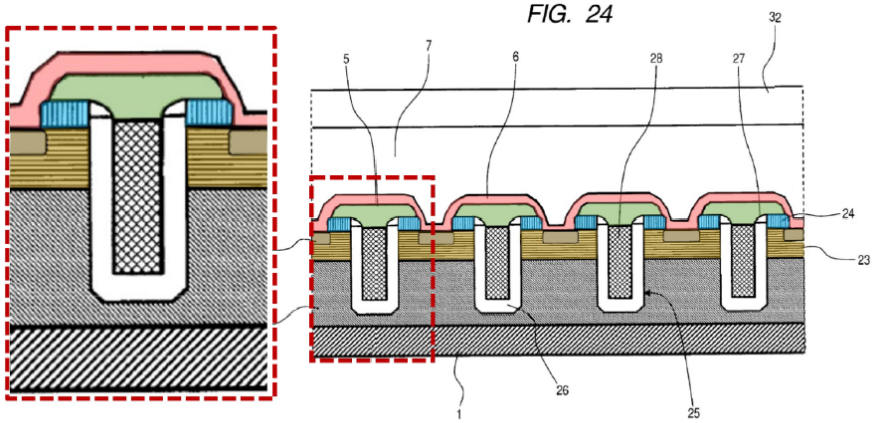
impossible." Prelim. Resp. 42. Dr. Banerjee's testimony indicates that Figure 5 is clear enough to adequately determine the relevant dimensions. *See* Ex. 1002 ¶¶ 147, 148. Patent Owner asserts it is not. This is a factual dispute best resolved with a full record at trial.

3. Obviousness of Claims 8 and 9 based on Sekiguchi and Hebert

Petitioner contends claims 8 and 9 would have been obvious over Sekiguchi and Hebert. Pet. 91–100. Based on Petitioner's analysis and for the reasons explained below, we find Petitioner has, at this stage, demonstrated a reasonable likelihood of prevailing on this challenge.

a. Petitioner's Proposed Combination of Herbert and Sekiguchi

According to Petitioner, Sekiguchi's Figure 24 (reproduced below, Petitioner's excerpt/annotation) includes claim 8's base layer (23, yellow) source layer (24, blue), insulating film (5, green), gate structures (28), conductive portion (6, pink), source electrode (7). Pet. 94–97; *see id*. at 97.



EX1044, Fig. 24 (annotated)

Element [8.7] requires "a dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other is 10 nm or more and 40 nm or less." According to Petitioner, although Sekiguchi's teaches the relevant dimension (the contact between the upper

surface of source layer 24 and conductive portion 6) is about 80 nm, "*Hebert* teaches this dimension can be as little as 20nm," which is within the claimed 10 to 40 nm range. *Id*. at 99. Petitioner explains that a skilled artisan would have found it obvious "to reduce Sekiguchi's stairstep from about 80nm to as little as 20nm to improve adhesion of the interlayer insulator." *Id*. at 92. Petitioner also contends its proposed combination of Sekiguchi and Hebert is

> [a]n example of (1) combining prior art elements (*Hebert*'s stair width and *Sekiguchi*'s device) according to known methods (BOE) to yield predictable results (enhanced contact resistance, maintaining durability); (2) substitution of one known element (*Hebert*'s stair width) for another (*Sekiguchi*'s stair width) to obtain predictable results (enhanced contact resistance, maintaining durability); (3) use of known technique (*Hebert*'s stairs width) to improve similar devices (*Sekiguchi*'s device) in the same way; and (4) a choice among a finite number of identified, predictable solutions (*Hebert*'s stair widths), with a reasonable expectation of success.

Id. at 93. Given this analysis, we agree with Petitioner that its proposed Sekiguchi-Hebert combination teaches each element in claim 8. In addition, Petitioner has articulated sufficient reasoning with rational underpinning to support the legal conclusion that its proffered combination would have been obvious to one skilled in the art. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

Patent Owner argues that Petitioner's obviousness challenge fails "because a POSITA would not have looked to Hebert to improve on Sekiguchi." Prelim. Resp. 55. This is so, according to Patent Owner, because Hebert teaches using only N-doped regions in field effect transistors, while Sekiguchi teaches using regions of alternating doping types, i.e., both N- and P- doped regions. Prelim. Resp. 56. According to

Patent Owner, "Hebert teaches a fundamentally different device structure and disparages mixing N and P body regions, making it unlikely that a POSITA would look to Hebert to improve on Sekiguchi." *Id*. In addition, according to Patent Owner, "Petitioner points to nothing which indicates that any purported improvement in adhesion would be worth the noted tradeoff of decreasing the metal-source contact area." Prelim. Resp. 57.

We disagree with Patent Owner's argument. To the extent Patent Owner is asserting Hebert and Sekiguchi are non-analogous art, clearly both are from the same field of endeavor as "both describe the same type of [MOSFET] device." Ex. 1002 ¶ 283. In addition, even if Patent Owner is correct that there would be a potential cost to substituting Hebert's 20nm step for Sekiguchi's 80nm step (i.e. decreasing the metal-source contact area), that tradeoff does not necessarily undermine Petitioner's proffered combination given Petitioner's articulated benefits, including improved adhesion and durability. *See* Pet. 92; *see also Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) ("The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another.").

b. Claim Element [8.7]

Element [8.7] requires "a dimension of a part in which the upper surface of said source layer and said conductive portion are in contact with each other is 10 nm or more and 40 nm or less." Ex. 1001, 14:13–16. Patent Owner criticizes Petitioner's reliance on Herbert because, Patent Owner explains, Hebert's source layer does not have a "second conductivity type,"

or a "conductive portion" as claim 8 requires. Prelim, Resp. 59. We disagree with Patent Owner's argument because it attacks the references individually rather than addressing the asserted combination, as set forth in the Petition. Petitioner relies on Hebert only for teaching claim 8's 10–40nm stair width. *See, e.g.*, Pet. 91–93 (describing using "*Hebert*'s stair width and *Sekiguchi*'s device"). Thus, it does not matter whether Herbert teaches the claimed second conductivity type or conductive portion because Petitioner relies on Sekiguchi, not Herbert, for teaching those features.

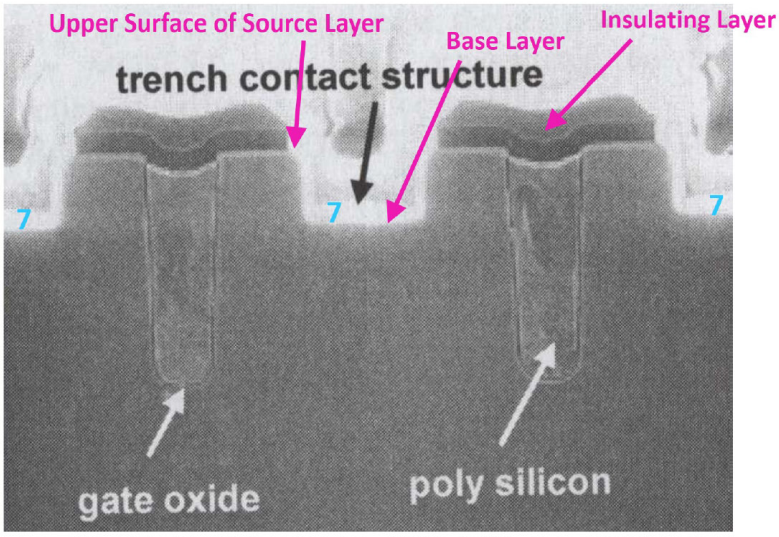
4. Obviousness of Claims 1–3 based on Kim03 and Sekiguchi

Petitioner contends claims 1–3 would have been obvious over Kim03 and Sekiguchi. Pet. 81–91. Based on Petitioner's analysis and for the reasons explained below, we find Petitioner has, at this stage, demonstrated a reasonable likelihood of prevailing on this challenge.

a. Claim Element [1.5]

Element [1.5] requires "a plurality of conductive portions penetrating said insulating film and said source layer and electrically connected to said source layer and said base layer." Ex. 1001 at 12:25–27. Patent Owner argues that Petitioner has not adequately accounted for the recited *plurality* of conductive portions because "Petitioner simply refers back to its Ground 2a analysis," which addresses a limitation requiring a single conductive portion, rather than "a plurality of conductive portions" as recited in Element [1.5]. Prelim. Resp. 49.

We disagree with Patent Owner's argument. Petitioner's Ground 2a analysis relies on Kim03's Figure 5 (reproduced below, Petitioner's annotations). Pet. 77–78.



EX1034, Fig. 5 (annotated)

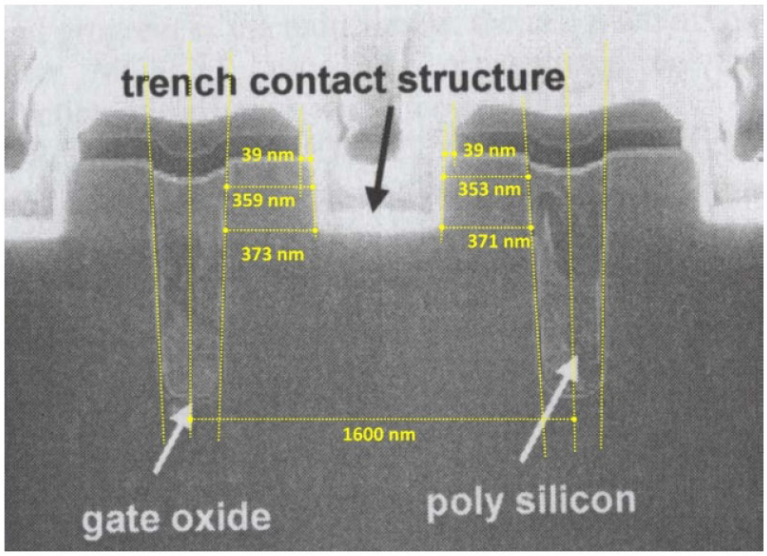
Id. at 78. In its Ground 2a analysis, Petitioner corresponds thin barrier metal 7 to the claimed conductive portion. *See id*. at 77. The figure above plainly shows both a single barrier metal 7 (the singular "conductive portion" needed for Ground 2a) and a plurality of barrier metal 7s (claim Element [1.5]'s "plurality of conductive portions"), without any additional explanation from Petitioner.

Next, Patent Owner challenges that thin barrier metal 7 fails to teach the claimed "conductive portions electrically connected to said source layer and said base layer" because Figure 5 does not clearly show where the barrier metal begins or ends or where it is electrically connected. Prelim. Resp. 50–51. We disagree with Patent Owner's argument. According to Dr. Banerjee, "Annotated Figure 5 . . . illustrates how the barrier metal (labeled '7') . . . contacts an upper surface of the source layer, and is electrically connected to the source and base layers." Figure 5 supports Dr. Banerjee's statement, even if the Figure's shading and boundary regions are less than perfectly clear. To the extent that Patent Owner contests Dr.

Banerjee's understanding of Figure 5, that is an issue best resolved on a full evidentiary record at trial.

b. Claim Element [1.9]

Element [1.9] requires "a dimension of a part in which said source layer and said base layer are in contact with each other between said gate structures and said conductive portions are 0.36 μm or more and 0.43 μm or less." Ex. 1001, 12:37–40. Petitioner asserts Kim03's Figure 5 depicts this claimed dimension because it teaches that Figure 5 has "unit cells with a cell pitch of 1.6 μm," which provides scale for Figure 5. *See* Pet. 80. Using that scale, Petitioner asserts Figure 5 (reproduced below, Petitioner's annotations) depicts the relevant surface as in a region that largely overlaps the claimed region. Pet. 87–88.



***Kim 2003* at Fig. 5 (annotated)**

Patent Owner argues that Petitioner's challenge fails because "[e]ven if Petitioner's measurements were accurate enough to estimate what range of dimensions Kim03 conceivably could have used, Petitioner concedes it has

no idea which value in its estimated range Kim03 would actually teach, and more than a third of its estimated range of possibilities falls outside of the claimed dimension." Prelim. Resp. 55. We disagree with Patent Owner's argument. Petitioner's expert, Dr. Banerjee provides two ranges for the conductive-portion dimensions: one 359 to 371 nm and the other 353 to 371 nm. Ex. 1002 ¶¶ 269, 270. Dr. Banerjee further testifies that "[f]or the source regions to sufficiently overlap with the gate structures and make a good device, a person of ordinary skill in the art would have understood the interface is located closer to the bottom of the contact trench (i.e., much closer to 371 nm or 373 nm) than to the top of the gate (i.e., to 359 nm or 353 nm)." Given this testimony, at this stage, Petitioner has shown sufficiently that the Kim03 teaches the claimed conductive-portion dimension between 0.36 and 0.43 μm.

5. Obviousness of Claims 1 and 3 based on Sekiguchi and Williams99

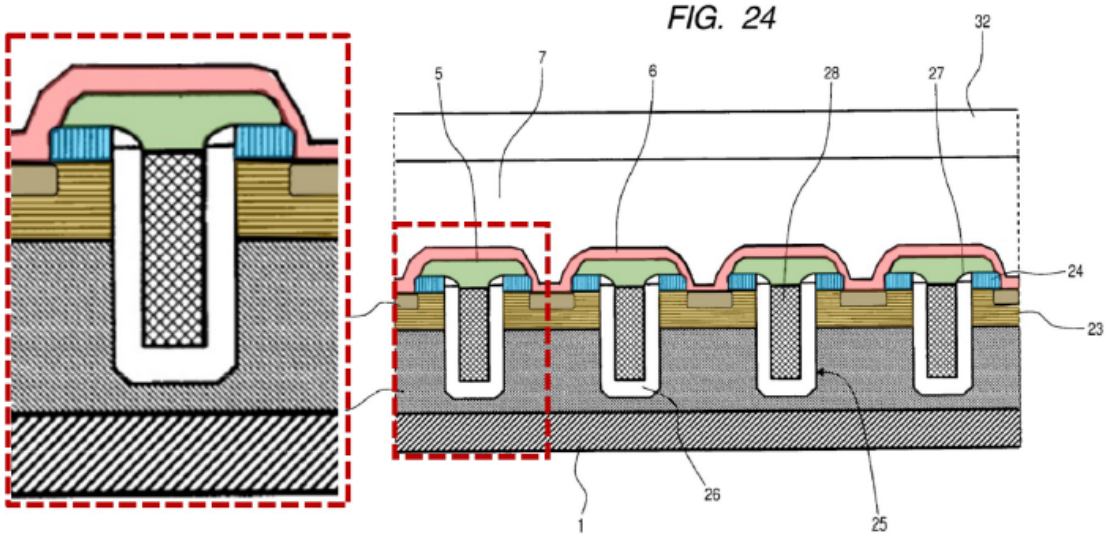
Petitioner contends claims 1 and 3 would have been obvious over Sekiguchi and Williams99. Pet. 100–107. Based on Petitioner's analysis and for the reasons explained below, we find Petitioner has, at this stage, demonstrated a reasonable likelihood of prevailing on this challenge.

a. Claim 1 Element [1.5]

Element [1.5] requires "a plurality of conductive portions penetrating said insulating film and said source layer and electrically connected to said source layer and said base layer." Ex. 1001, 12:25–27. Similar to its argument above, Patent Owner argues that Petitioner has not adequately accounted for the recited *plurality* of conductive portions because "Petitioner simply refers back to its Ground 3a analysis," which addresses a limitation

requiring a single conductive portion, rather than "a plurality of conductive portions" as recited in Element [1.5]. Prelim. Resp. 60.

We disagree with Patent Owner's argument. Petitioner's Ground 3a analysis relies on Sekiguchi's Figure 24 (reproduced below, Petitioner's excerpt and annotations). Pet. 96–97.



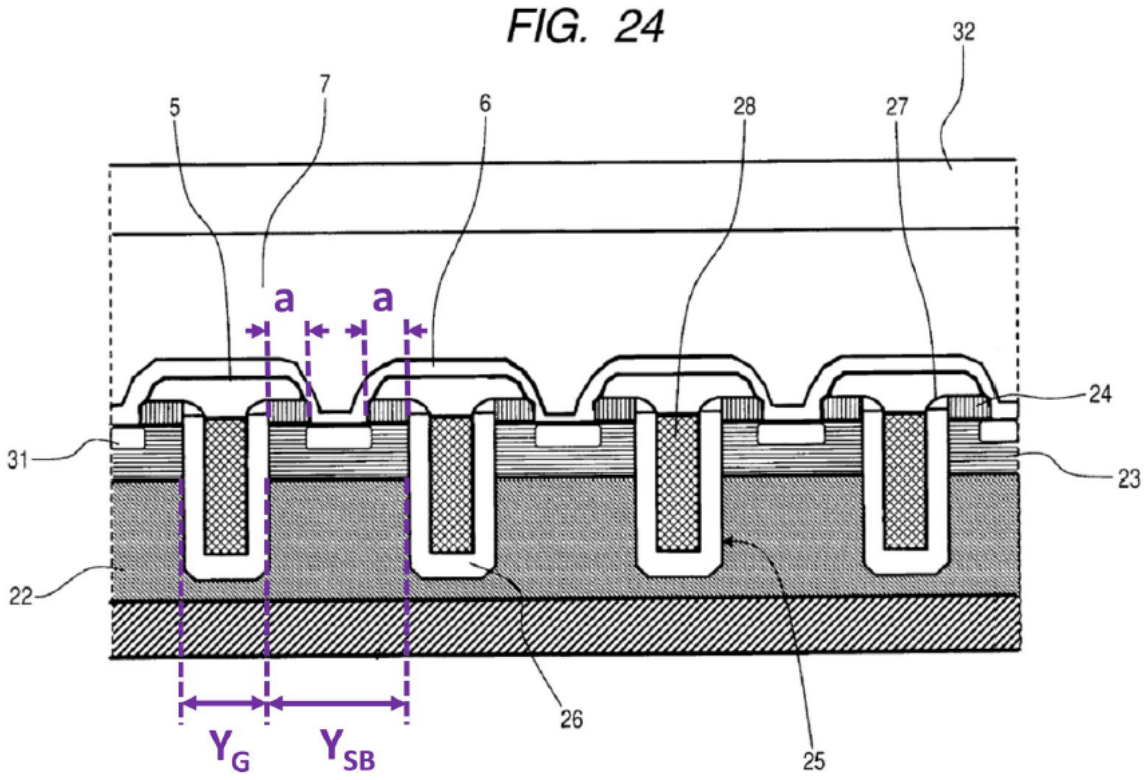
EX1044, Fig. 24 (annotated)

In its Ground 3a analysis, Petitioner corresponds TiW film 6 to the claimed conductive portion. *See id*. at 77. The figure above plainly shows both a single TiW film 6 portion (the singular "conductive portion" needed for Ground 3a) and a plurality of TiW film 6 portions (claim Element [1.5]'s "plurality of conductive portions"), without any additional explanation from Petitioner.

b. *Claim Element [1.9]*

Element [1.9] requires "a dimension of a part in which said source layer and said base layer are in contact with each other between said gate structures and said conductive portions are 0.36 μm or more and 0.43 μm or less." Ex. 1001, 12:37–40. Petitioner suggests that the claimed mesa-trench

width corresponds to dimension "a" in Sekiguchi's Figure 24, reproduced below with Petitioner's annotations.



EX1044, Fig. 24 (annotated)

Pet. 106. According to Petitioner, while Sekiguchi does not disclose dimension "a," given a skilled artisan's knowledge and the available technology at the time of the invention, one reading Williams99 would have understood it to suggest dimension "a" within the claimed 0.36–0.43 μm range for devices with Sekiguchi's geometry and dimensions. *See id*. 101–103. In particular, Petitioner contends its proposed combination of Sekiguchi and Williams99 is

> an example of (1) combining prior art elements (*Sekiguchi*'s device and *Williams99*'s dimensions) according to known processing methods to yield predictable results (better on-resistance and smaller devices); (2) use of known technique

> (*Williams99*'s dimensions) to improve similar devices (*Sekiguchi*'s device) in the same way; and (3) a teaching, suggestion, or motivation in the prior art (*Williams99*'s dimensions) that would have led a POSITA to implement *Sekiguchi*'s device using the claimed dimensions.

Id.

Patent Owner argues that Petitioner's obviousness challenge fails for a number of reasons, none of which we find persuasive. *See* Prelim. Resp. 61–61. For example, although Patent Owner does not contest the prior art teaches the claimed 0.36–0.43μm dimension, Patent Owner notes that according to Williams99, smaller, realistically feasible dimensions below the claimed range would result in even better performance. *See* Prelim. Resp. 66–67. Patent Owner argues a skilled artisan would not have "arbitrarily selected" the claimed range, but instead would have sought to make the claimed dimension as small as possible, thus "resulting in a contact region outside the claimed dimension." *Id*. at 67. We disagree with Patent Owner's argument because Petitioner does not need to demonstrate that the "prior art suggests that the combination claimed" in the patent "is the preferred, or most desirable, combination." *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004); *see Merck & Co., Inc. v. Biocraft Labs.*, Inc., 874 F.2d 804, 807 (Fed. Cir. 1989) (noting that in an obviousness inquiry "all disclosures of the prior art, including unpreferred embodiments, must be considered").

Given Petitioner's analysis outlined above, we agree with Petitioner that its proposed combination of Sekiguchi's device with Williams99's dimensions suggests Element [1.9]. *See* Pet. 105–107. In addition, Petitioner has articulated sufficient reasoning with rational underpinning to support the legal conclusion that its proffered combination would have been

obvious to one skilled in the art. *See* Pet. 100–103; *see also KSR*, 550 U.S. 398, 418.

6. Undisputed Limitations

As for the remaining limitations of independent claims 1, 4, and 8, Petitioner provides a detailed analysis of how the prior art disclosures teach every element of those challenged claims. Other than as discussed above, Patent Owner does not additionally challenge Petitioner's analysis in its Preliminary Response. We have reviewed Petitioner's arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its challenges to independent claims 1, 4, and 8.

7. Petitioner's Undisputed Obviousness Grounds

Petitioner challenges dependent claims 2, 3, 5–7, and 9 as outlined in Section II.C above. Other than as discussed above, Patent Owner does not additionally challenge Petitioner's analysis in its Preliminary Response. We have reviewed Petitioner's arguments and the underlying evidence cited in support and are persuaded that, at this stage, Petitioner sufficiently demonstrates that dependent claims 2, 3, 5–7, and 9 are invalid over the asserted prior art.

V. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition. We decline also to exercise our discretion to deny institution under 35 U.S.C. § 314(a).

VI. ORDER

Accordingly, it is:

ORDERED that *inter partes* review of claims 1–9 of the '867 patent is instituted on all grounds in the Petition;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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