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Paper 64
Date: March 9, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

TELA INNOVATIONS, INC.,
Patent Owner.

IPR2019-01520
Patent 10,186,523 B2

Before JO-ANNE M. KOKOSKI, KRISTINA M. KALAN, and WESLEY B. DERRICK, *Administrative Patent Judges.*

KOKOSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)
Dismissing Patent Owner's Motion to Exclude
37 C.F.R. § 42.64(c)

I. INTRODUCTION

We have jurisdiction to conduct this *inter partes* review under 35 U.S.C. § 6, and this Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Intel Corporation ("Petitioner") has not shown by a preponderance of the evidence that claims 1, 2, 8–12, 25, and 26 ("the challenged claims") of U.S. Patent No. 10,186,523 B2 ("the '523 patent," Ex. 1001) are unpatentable.

A. Procedural History

Petitioner filed a Petition to institute an *inter partes* review of claims 1, 2, 8–12, 25, and 26 of the '523 patent. Paper 2 ("Pet.). Tela Innovations, Inc. ("Patent Owner") filed a Preliminary Response. Paper 9. With Board authorization, Petitioner filed a Preliminary Reply (Paper 11), and Patent Owner filed a Preliminary Sur-Reply (Paper 12). Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of claims 1, 2, 8–12, 25, and 26 on the ground advanced in the Petition. Paper 14, 11, 31.

After institution of trial, Patent Owner filed a Patent Owner Response ("PO Resp.," Paper 32 (confidential), 36 (public)), Petitioner filed a Reply ("Pet. Reply," Paper 43 (confidential), 46 (public)), and Patent Owner filed a Sur-Reply ("PO Sur-Reply," Paper 47 (confidential), 50 (public)). Patent Owner filed a Motion to Exclude Exhibit 1068, Exhibit 1071, and paragraphs 81–83, 90, and 91 of Exhibit 1062. Paper 54. Petitioner filed an Opposition (Paper 56), and Patent Owner filed a Reply (Paper 57).

An oral hearing was held on December 9, 2020, and a transcript is included in the record. Paper 62 (Tr.).

B. Related Proceedings

The parties indicate that the '523 patent is the subject of an investigation at the International Trade Commission, Inv. No. 337-TA-1148,

and a civil action in the Northern District of California, *Intel Corp. v. Tela Innovations, Inc.*, Case No. 3:18-cv-02848-WHO (N.D. Cal.) ("the NDCA Action"). Pet. 1–2; Paper 5, 2. The parties also identify several other civil actions in which the '523 patent is asserted. Pet. 3; Paper 5, 2–3.

The '523 patent is the subject of IPR2019-01521 and IPR2019-01522, also filed by Petitioner. Paper 5, 3. The parties further identify several *inter partes* review proceedings involving patents related to the '523 patent. Pet. 4; Paper 5, 3.

C. The '523 Patent

The '523 patent, titled "Semiconductor Chip Having Region Including Gate Electrode Features Formed in Part from Rectangular Layout Shapes on Gate Horizontal Grid and First-Metal Structures Formed in Part from Rectangular Layout Shapes on at Least Eight First-Metal Gridlines of First Metal Vertical Grid," is directed to "a dynamic array architecture" that addresses "semiconductor manufacturing process variability associated with a continually increasing lithographic gap." Ex. 1001, code (54), 7:7–10. The '523 patent defines lithographic gap "as the difference between the minimum size of a feature to be defined and the wavelength of light used to render the feature in the lithographic process, wherein the feature size is less than the wavelength of the light." *Id.* at 7:10–15.

The '523 patent explains that "[c]urrent lithographic processes utilize light wavelength of 193 nm," but that "current feature sizes are as small as 65 nm and are expected to soon approach sizes as small as 45 nm." Ex. 1001, 7:15–18. Because the interaction radius of light is about five wavelengths, "shapes exposed with a 193 nm light source will influence the exposure of shapes approximately 5*193 nm (965 nm) away," such that "approximately two times as many 65 nm size features may be within

the 965 nm interaction radius" as compared to larger (i.e., 90 nm) sized features. *Id.* at 7:20–28. "Due to the increased number of features within the interaction radius of the light source, the extent and complexity of light interference contributing to exposure of a given feature is significant." *Id.* at 7:29–32. The '523 patent explains that parametric failures introduced by, for example, "arbitrary two-dimensionally varying figures disposed in proximity to each other" "may result from failure to accurately print contacts and vias and from variability in fabrication processes." *Id.* at 8:16–24.

The '523 patent describes a dynamic array architecture that "is defined to address" semiconductor manufacturing process variability that results from an increasing lithographic gap. Ex. 1001, 8:28–30. Figure 2, reproduced below, illustrates a generalized stack of layers used to define a dynamic array architecture.

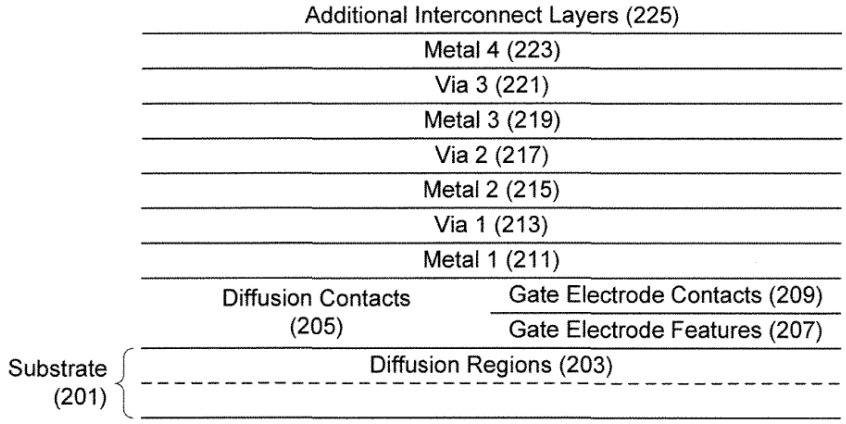

Fig. 2

Figure 2 depicts the underlying structure of a dynamic array according to one embodiment described in the '523 patent. *Id.* at 5:53–55, 9:14–16. The dynamic array is built up in layers upon base substrate 201, in which diffusion regions 203 are defined. *Id.* at 9:31–34. Diffusion regions 203

represent selected regions of base substrate 201 "within which impurities are introduced for the purpose of modifying the electrical properties" of base substrate 201. *Id.* at 9:34–38. Diffusion contacts 205 are defined above diffusion regions 203 in order to enable connection between diffusion regions 203 and conductor lines (not depicted in Figure 2). *Id.* at 9:38–40. Gate electrode features 207 are defined above diffusion regions 203 to form transistor gates, and gate electrodes 209 are defined to enable connection between gate electrode features 207 and conductor lines. *Id.* at 9:43–47. Interconnect layers that include first metal layer 211, first via layer 213, second metal layer 215, second via layer 217, third metal layer 219, third via layer 221, and fourth metal layer 223 are defined above diffusion contacts 205 and gate electrode features 207. *Id.* at 9:50–56. The metal and via layers enable definition of the desired circuit connectivity. *Id.* at 9:56–57.

Figure 5 of the ’523 patent, reproduced below, illustrates an example layout of elements of a dynamic array.

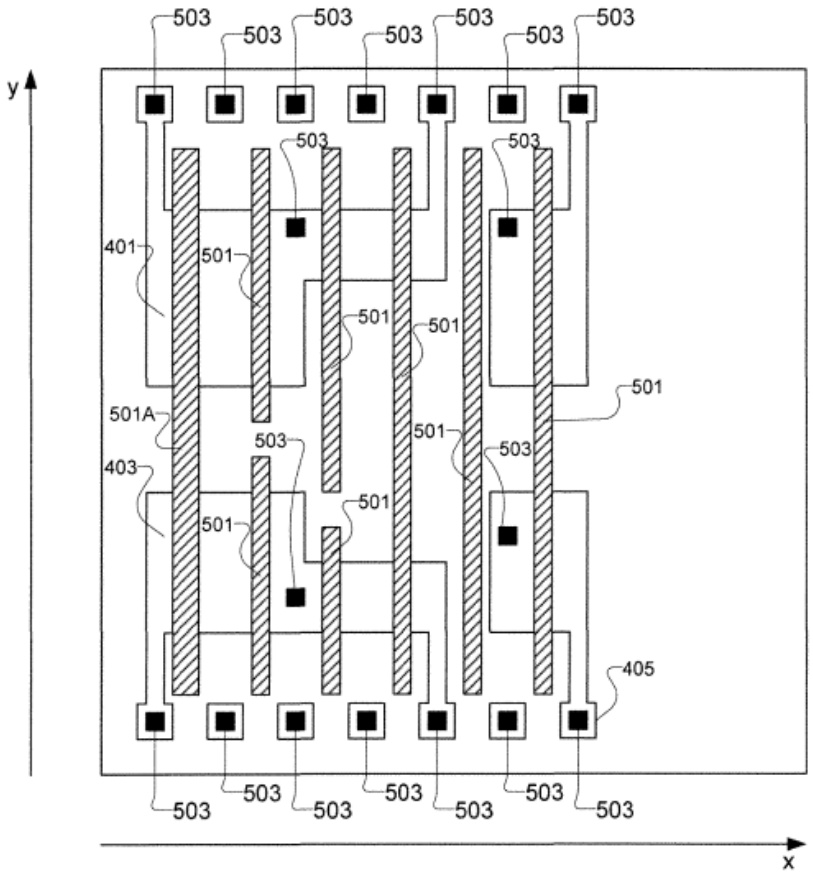

Fig. 5

Figure 5 shows an example layout of elements of a dynamic array including a gate electrode layer, a diffusion contact layer, and a diffusion layer. *Id.* at 14:20–23. Gate electrodes 501 are defined as linear shaped features extending in a parallel relationship across the dynamic array in the “y” direction. *Id.* at 14:25–28. Gate electrode features 501 form n-channel and p-channel transistors as they cross diffusion regions 403 and 401, respectively. *Id.* at 14:40–42. The ’523 patent explains that each of the gate electrode tracks may be interrupted any number of times in linearly traversing across the dynamic array in order to provide required electrical

connectivity for a particular logic function. *Id.* at 14:51–54. Diffusion contacts 503 are defined at each diffusion square 405 to enhance the printing of diffusion contacts via resonant imaging. *Id.* at 15:15–17. Gate electrode features 501 and diffusion contacts 503 share a common grid spacing. *Id.* at 15:21–22.

Figure 6 of the '523 patent, reproduced below, shows another example layout of elements of a dynamic array, adding a gate electrode contact layer to the structure of Figure 5.

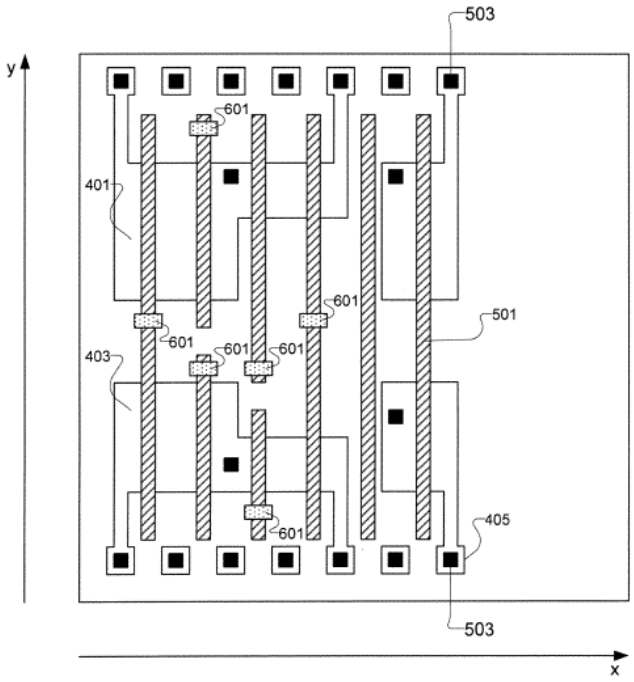

Fig. 6

Figure 6 illustrates elements of a dynamic array, including a gate electrode layer defined above and adjacent to the gate electrode layer depicted in Figure 5 above. *Id.* at 15:45–48. Gate electrode contacts 601 enable connection of gate electrode features 501 to the overlying metal conduction lines. *Id.* at 15:48–51. Gate electrode contacts 601 are "oversized in the direction perpendicular to the gate electrode features 501 to ensure overlap

between the gate electrode contact 601 and the gate electrode feature 501." *Id.* at 15:59–63.

Figure 8A of the '523 patent, reproduced below, illustrates another example layout of elements of a dynamic array.

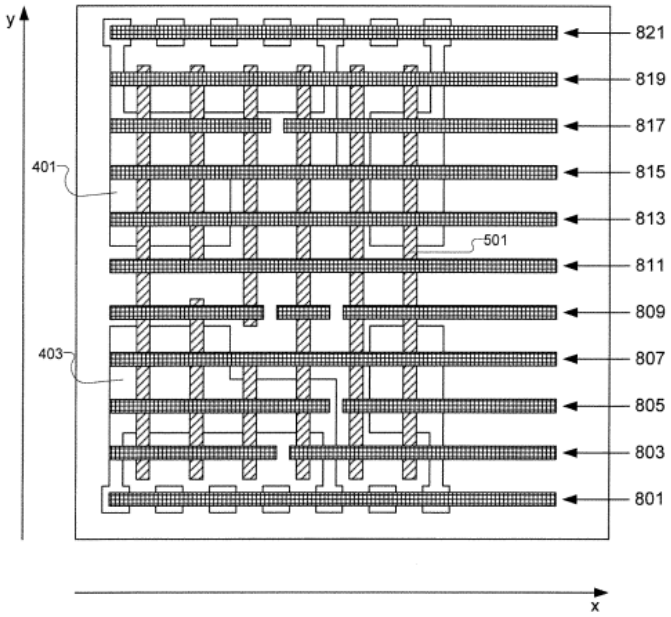

Fig. 8A

Figure 8A shows metal layer 1 defined above the gate electrode layer depicted in Figure 6 above. Ex. 1001, 16:36–38. Metal layer 1 includes a number of metal 1 tracks 801–821 defined to include linear shaped features extending in a parallel relationship across the dynamic array. *Id.* at 16:38–41. Metal 1 tracks 801–821 extend in a direction substantially perpendicular to gate electrode features 501, and, thus, extend linearly in the "x" direction. *Id.* at 16:41–46. Each of metal 1 tracks 801–821 may be interrupted any number of times in linearly traversing across the dynamic array to provide for electrical connectivity for a particular logic function to be implemented. *Id.* at 16:53–57. The '523 patent explains that "[t]he metal 1 track pattern is optimally configured to optimize the use of 'white space' (space not

occupied by transistors)." *Id.* at 17:20–22. In Figure 8A, metal 1 tracks 803, 809, 811, and 819 are defined as gate electrode contacts in order to minimize white space. *Id.* at 17:24–26. Metal 1 tracks 805 and 807 connect to n-channel transistor source and drains, and metal 1 tracks 813, 815, and 817 connect to p-channel source and drains. *Id.* at 17:26–29.

D. Challenged Claims

Petitioner challenges claims 1, 2, 8–12, 25, and 26 of the '523 patent. Claim 1, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

> 1. A semiconductor chip, comprising
>
> gate electrode features formed within a region of the semiconductor chip, the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process, the gate electrode feature layout shapes positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein all gate gridlines extend in a y-direction, wherein adjacent gate gridlines are separated from each other by a gate pitch, each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second

transistor type and does not form a gate electrode of a transistor of the first transistor type;

at least six gate contact structures formed within the region of the semiconductor chip, the at least six gate contact structures formed in part utilizing corresponding at least six gate contact structure layout shapes as an input to a lithography process, wherein at least six gate electrode features within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six gate contact structures, each of the at least six gate contact structure layout shapes having a substantially rectangular shape with a corresponding length greater than a corresponding width and with the corresponding length oriented in an x-direction, each of the at least six gate contact structure layout shapes positioned and sized to overlap both edges of the gate electrode feature layout shape corresponding to the gate electrode feature to which it is in physical and electrical contact; and

a first metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material, wherein the first-metal layer includes first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, wherein the first-metal structure layout shapes are positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, wherein all first-metal gridlines extend in the x-direction, wherein at least eight of the at least eight first-metal gridlines have at least one first-metal structure layout shape positioned thereon, each first-metal structure layout shape in the region having a substantially

rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner on an associated first-metal gridline;

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit, wherein electrical connections within the logic circuit collectively include at least five first-metal structures corresponding to at least five first-metal structure layout shapes respectively positioned on at least five different first-metal gridlines,

wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding diffusion region, wherein some diffusion regions within the region of the semiconductor chip are physically and electrically contacted by at least one diffusion contact structure, the at least one diffusion contact structure formed in part utilizing corresponding at least one diffusion contact structure layout shape as an input to a lithography process, each diffusion contact structure layout shape within the region positioned in a substantially centered manner along an associated diffusion contact gridline of a diffusion contact grid, the diffusion contact grid having a diffusion contact gridline-to-diffusion contact gridline spacing measured in the x-direction equal to the gate pitch.

Ex. 1001, 24:50–26:4.

E. Prior Art and Asserted Ground

Petitioner challenges the patentability of claims 1, 2, 8–12, 25, and 26 of the ’523 patent under 35 U.S.C. § 103[1] as obvious over the combined

[1] The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the effective filing date of the ’523 patent is before March 16, 2013, the effective date of the relevant amendment, the pre-AIA version of § 103 applies.

teachings of Yano,[2] Kitabayashi,[3] and Ikoma.[4] Pet. 7. Petitioner relies on the Declarations of Stanley Shanfield, Ph.D. (Ex. 1002, Ex. 1062) in support of its contentions. Patent Owner relies on the Declarations of Mr. Scott Baker (Ex. 2040) and Dr. Sunil P. Khatri (Ex. 2074).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art ("POSITA") "would have been a person having a Bachelor's degree in Electrical Engineering, Physics or Materials Science with three to five years of industry experience in semiconductor [integrated circuit] design, layout or fabrication." Pet. 17 (citing Ex. 1002 ¶¶ 53–56). Petitioner further contends "[a]dditional education might compensate for less experience, and vice-versa." *Id*. Patent Owner, through its declarant, Dr. Khatri, argues that a POSITA would have had either a Bachelor's degree in electrical engineering and "five years of experience in semiconductor layout technology and integrated circuit design;" a Master's degree in electrical engineering and "three years of experience in the same field;" or "comparable experience." Ex. 2074 § 78; *see also* PO Resp. 9–10 (stating that Patent Owner "has proposed a different definition of a POSITA" than Petitioner). Patent Owner also "maintains that the Challenged Claims are not obvious under either definition of a POSITA." PO Resp. 10 (citing Ex. 2074 ¶ 79). Neither party argues that the outcome of this case would differ based on our adoption of any particular definition of one of ordinary skill in the art.

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[2] US Patent No. 7,538,368 B2, issued May 26, 2009 (Ex. 1011).
[3] US Patent No. 7,200,831 B2, issued Apr. 3, 2007 (Ex. 1016).
[4] US Patent No. 7,279,727 B2, issued Oct. 9, 2007 (Ex. 1017).

On this record, we find that the differences in the parties' contentions as to the level of ordinary skill set forth by both Petitioner and Patent Owner are based on a Bachelor's degree in electrical engineering and a length and type of experience that overlap. We adopt Patent Owner's definition, which overlaps that set forth by Petitioner, particularly regarding a Bachelor's degree in electrical engineering, with five years of experience in semiconductor layout technology and integrated circuit design, and because it is consistent with the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that "specific findings on the level of skill in the art . . . [are not required] 'where the prior art itself reflects an appropriate level and a need for testimony is not shown.'" (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))). Our determination regarding the patentability of the challenged claims does not turn on the differences between Petitioner's and Patent Owner's definitions, and we note that our conclusions would be the same under either assessment.

B. Claim Construction

We apply the claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2019). Under *Phillips*, the "words of a claim 'are generally given their ordinary and customary meaning,'" which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1312–13. "[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d

1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Petitioner contends that "the Board does not need to construe any claim term for purposes of evaluating the prior art in this Petition." Pet. 17–18. Petitioner does, however, provide constructions of the terms "gate electrode," "gate electrode feature(s)," and "gate contact structure(s)" that were proposed by the parties in the NDCA Action. *Id.* at 18. Patent Owner points to the Claim Construction Order from the NDCA Action, and states that Patent Owner "applies the District Court's constructions" in the present proceeding, but does not propose any express constructions of its own. PO Resp. 10 (citing Ex. 2093, 11, 14, 16).

On the full record now before us, we determine it is not necessary to construe any claim term expressly to resolve the parties' dispute. *Nidec Motor*, 868 F.3d at 1017.

C. Alleged Obviousness Over Yano, Kitabayashi, and Ikoma

Petitioner contends that claims 1, 2, 8–12, 25, and 26 are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combined teachings of Yano, Kitabayashi, and Ikoma. Pet. 25–95.

1. Overview of Yano

Yano "relates to a standard cell used in a semiconductor integrated circuit, a standard cell library, and a semiconductor integrated circuit using it, and particularly relates to a layout structure thereof." Ex. 1011, 1:16–19. Yano explains that the "miniaturization of semiconductor integrated circuits in recent years" has led to "a problem of variation in final dimension of various patterns," and that "variation in final dimensions of gates of transistors affects transistor characteristics severely." *Id.* at 1:24–28. Yano, therefore, describes its objective as "suppressing variation in characteristics

of a standard cell even with irregularity in gate length of gates or dummy gates." *Id.* at 4:44–46.

Yano describes a standard cell according to the invention that has a plurality of transistors, each having a diffusion region, a gate, and at least one intra-cell dummy gate on a side of the standard cell. *Id.* at 5:43–46. The plurality of transistors include at least one transistor adjacent to the intra-cell dummy gate that is in an OFF state. *Id.* at 5:46–48. Yano teaches that the "[t]he gate length of the intra-cell dummy gate is determined by the dummy gate provided on the edge of the standard cell and the dummy gate provided on the edge of the adjacent cell." *Id.* at 5:49–51. If the length of the intra-cell dummy gate is different from the gate length of the gates in the adjacent standard cell, "the characteristics of the gate adjacent to the intra-cell dummy gate varies from the characteristics of the other gates." *Id.* at 5:52–56. Yano explains that, "[i]n the present invention, however, the transistor in the OFF state that does not contribute to the operation of the standard cell is adjacent to the intra-cell dummy gate, suppressing variation in the characteristics of the standard cell." *Id.* at 5:56–59.

Yano's Figure 4, which describes Yano's fourth embodiment, is reproduced below:

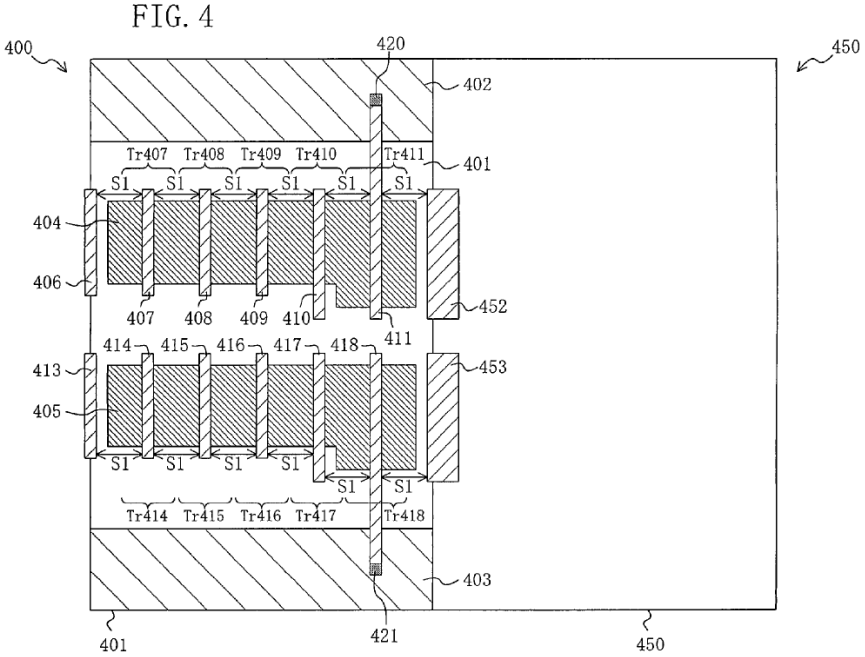


Figure 4 is a plan view of standard cell 400 described in Yano's fourth embodiment, with space for another standard cell 450 provided beside it. *Id*. at 11:65–12:1. Standard cell 400 includes: gates 407–411 in p-type diffusion region 404; gates 414–418 in n-type diffusion region 405; dummy gates 406 and 452 on the respective sides of p-type diffusion region 404 with spacing S1 from gates 407 and 411, respectively; dummy gates 413 and 453 on the respective sides of n-type diffusion region 405 with spacing S1 from gates 414 and 418, respectively; contact via 420 that connects gate 411 to source wiring 402; and contact via 421 that connects gate 418 to ground wiring 403. *Id*. at 12:8–28.

Dummy gates 452 and 453, located on the boundary between standard cells 400 and 450, are constituted by overlaying dummy gates located on the boundary of the right side of standard cell 400 with the dummy gates located

on the boundary of the left side of standard cell 450, and are shared by standard cells 400 and 450. *Id*. at 12:1–7. Yano explains that the dummy gate located on the boundary on the right side of standard cell 400 has the same gate length as gate 411, while the dummy gate located on the boundary of the left side of standard cell 450 has gate length larger than gate 411, so that when the dummy gates of standard cells 400 and 450 are overlaid with each other, the gate length of dummy gates 452 and 453 becomes larger than the gate length of gate 411 in standard cell 400. *Id*. at 12:46–53. Yano further explains that, in this embodiment, the final dimension of gates 411 and 418 adjacent to dummy gates 452 and 453 varies. *Id*. at 12:61–62. According to Yano, gates 411 and 418 "are fixed to the source potential and ground potential respectively to set the transistors Tr411, Tr418 to be in the OFF state," so that "possible variation in gate length of the gates 411, 418 does not affect the characteristics of the standard cell 400." *Id*. at 12:63–67.

Yano's Figure 5, which describes Yano's fifth embodiment, is reproduced below:

FIG. 5

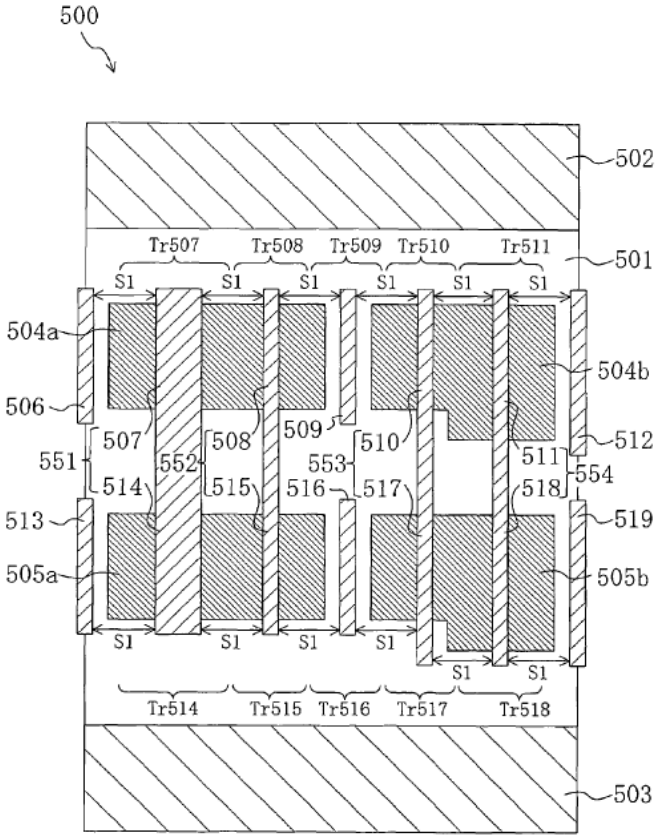


Figure 5 is a plan view of standard cell 500 described in Yano's fifth embodiment. *Id*. at 13:36–37. Standard cell 500 includes: p-type diffusion regions 504a and 504b; n-type diffusion regions 505a and 505b; conductive films 551 and 552 provided over p-type diffusion region 504a and n-type diffusion region 505a; conductive film 553 and 554 provided over p-type diffusion region 504b and n-type diffusion region 505b; dummy gates 506, 509, and 512 provided on the sides of p-type diffusion regions 504a and 504b; and dummy gates 513, 516, and 519 provided on the sides of n-type diffusion regions 505a and 505b. *Id*. at 13:40–56. Yano explains that

> [t]he conductive film 551 serves as a gate 507 on the p-type diffusion region 504*a* and as a gate 514 on the n-type diffusion region 505*a* while the conductive film 552 serves as a gate 508 on the p-type diffusion region 504*a* and as a gate 515 on the n-type diffusion region 505*a*. The conductive film 553 serves as a gate 510 on the p-type diffusion region 504*b* and as a gate 517 on the n-type diffusion region 505*b* while the conductive film 554 serves as a gate 511 on the p-type diffusion region 504*b* and as a gate 518 on the n-type diffusion region 505*b*.

Id. at 13:57–66.

Yano further explains that gates 507 and 514 in standard cell 500 "have gate length larger than that of the other gates," which "yields variation in final gate dimension of the gates 508, 515 adjacent to the gates 507, 514." *Id*. at 14:14–18. Yano teaches that standard cell 500 has a circuit of four inverters depicted in Yano's Figure 12A (not shown), and the inverter that drives the output pin "corresponds to the p-channel transistor 511 and n-channel transistor 518." *Id*. at 12:37–39, 14:21–24. Yano also teaches that "[a] characteristic of a transistor for driving an output pin affects the characteristics of a standard cell, especially, a delay characteristic of the standard cell." *Id*. at 14:18–21. Therefore, according to Yano,

> possible variation in final dimension of the gates 508, 515 less affects the delay characteristic of the standard cell 500. With a transistor having larger gate length than that of the other transistors, variation in characteristics of the standard cell can be suppressed by using a transistor which is located therearound and in final gate dimension as a transistor that does not drive the output pin.

Id. at 14:24–31.

2. Overview of Kitabayashi

Kitabayashi "relates to a semiconductor integrated circuit wiring design method, and a semiconductor integrated circuit." Ex. 1016, 1:15–17.

Kitabayashi explains that, "in the field of semiconductor integrated circuits, which will be more and more miniaturized, there is a strong demand for a wiring method that can improve the processing accuracy and controllability." *Id.* at 2:18–21. To that end, Kitabayashi describes a method of designing wiring of a semiconductor integrated circuit that includes, as a wiring base, at least two basic wiring pattern layers constituting a multilayer structure, each having: a plurality of wiring traces in a strip shape; a basic via array layer located between the two basic wiring pattern layers; and another basic array layer located at a side of one of the two basic wiring pattern layers. *Id.* at 2:33–47.

Kitabayashi explains that the wiring portion "is formed of a plurality of stacked wiring layers (processed wiring layers)," each of which is formed by cutting and/or removing "the wiring traces and vias of a basic wiring layer, on which a basic pattern (wiring traces in strip shapes and vias in pillar shapes) is formed before adopting a design, so that a regular density is obtained." *Id.* at 5:15–22. Kitabayashi teaches that "the wiring traces of a layer and those of its upper or lower layer cross each other in an orthogonal manner or an inclined manner, resulting in that when viewed two-dimensionally, the wiring traces constitute a grid." *Id.* at 5:54–58.

Kitabayashi further explains that "wiring traces are formed in advance with regularity, and vias are formed in an array," and, "[w]hen wiring is formed, some of the wiring traces and vias are used, and some of the wiring traces and vias not used for the actual wiring are left to remain so as to form a dummy pattern." *Id.* at 7:43–47. According to Kitabayashi, it is therefore "possible to actually perform a manufacturing process with such a redundant layout pattern necessary for miniaturization process, thereby improving the

controllability in the miniaturization process, and improving the yield." *Id.* at 7:47–51.

3. Overview of Ikoma

Ikoma "relates to a semiconductor device having a miniaturized transistor, and particularly to a measure against an optical proximity effect." Ex. 1017, 1:14–16. Ikoma explains that "[a]mong determinants of a transistor, the gate length is a particularly important determinant which defines the operation of the transistor," and, "[a]s the transistor is reduced in size, the gate length has been becoming much shorter and the variations in the gate length have been widening." *Id*. at 1:23–29. As a result, Ikoma explains, "the variations in propagation delay time have also widened and the design margin has increased, and thereby it has become difficult to provide" a semiconductor integrated circuit "having high performance." *Id.* at 1:29–32. Thus, Ikoma states that "[t]he object of the present invention is to provide a structure of a semiconductor device which can suppress variations in gate length caused by an optical proximity effect and realize an [semiconductor integrated circuit] having high performance even in a miniaturization process." *Id.* at 2:58–62.

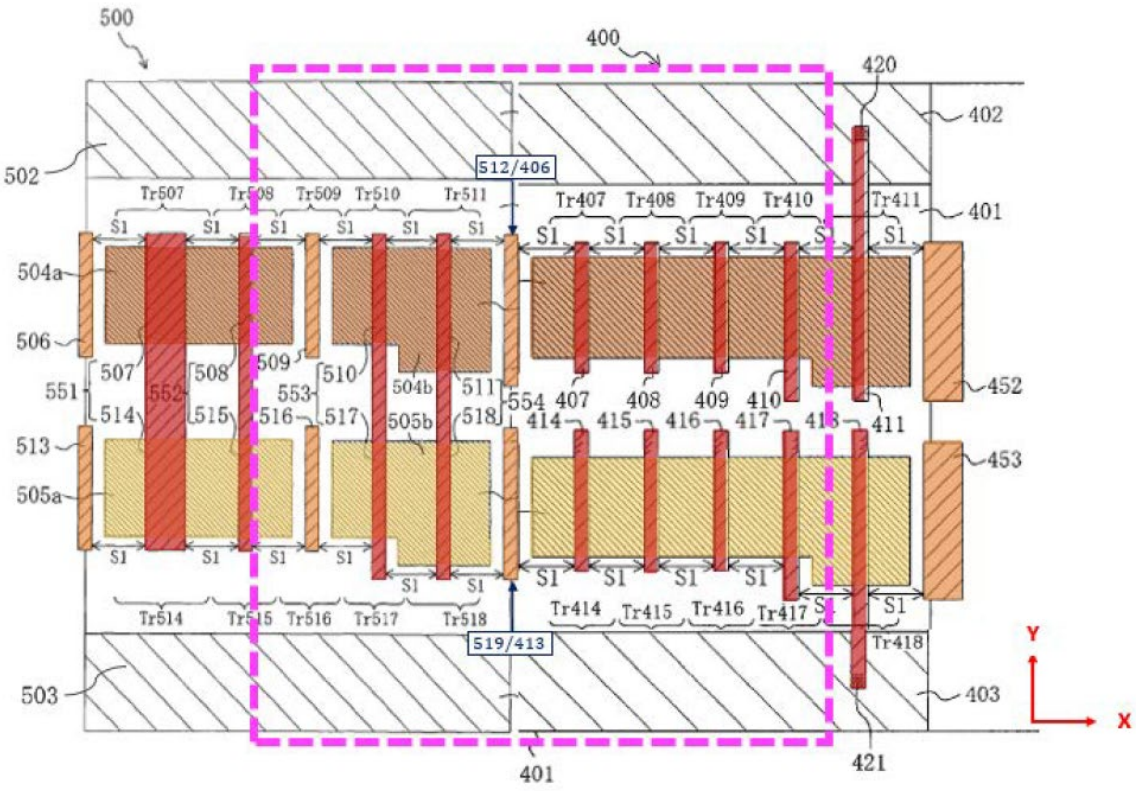
Ikoma describes a semiconductor device that "is provided with a gate conductor film of constant dimension in the gate length direction including a gate electrode part located on a diffusion region and a gate interconnect part located on an element isolation region." *Id.* at 2:63–67. Ikoma teaches that "the dimension of the gate contact in the gate length direction is larger than that of the gate interconnect part in the gate length direction." *Id.* at 2:67–3:3. Ikoma also teaches that "the gate conductor film has no reflex angle in the plan geometry," which "provides a semiconductor device which can suppress variations in the gate length of a MIS transistor caused by the

optical proximity effect." *Id.* at 3:4–8. Ikoma further teaches that "a conductor pad having a larger plane area than the gate contact may be further provided on each gate interconnect part to bring the gate contact into contact with the conductor pad." *Id*. at 3:33–37. According to Ikoma's invention, "it is possible to suppress variations in gate length of various MIS transistors caused by the generation of the optical proximity effect in the photolithographic step of the MIS transistors," and, therefore, "the design margin can be reduced" and a semiconductor integrated circuit "having high performance can be provided." *Id.* at 3:41–46.

4. Analysis

Petitioner contends, with supporting testimony from Dr. Shanfield, that the combined teachings of Yano, Kitabayashi, and Ikoma teach or suggest all of the limitations of the challenged claims (Pet. 30–95; Ex. 1002 ¶¶ 104–174, 201–223, 286–294), and "[c]ombining the teachings of Yano, Kitabayashi and Ikoma would have involved routine implementation, and posed no technical risks given their complementary teachings, and would have achieved the predictable benefits of improving performance and end-to-end manufacturability" (*id*. at 25 (citing Ex. 1002 ¶ 96)).

Petitioner's contentions are based on Petitioner's hypothetical combination and modification of the standard cells depicted in Yano's Figure 4 and Figure 5 to create Figure 4+5, reproduced below:



Yano Figure 4+5

Petitioner explains that Figure 4+5 "illustrates standard cells 400 and 500 in Yano Figures 4 and 5 laid out side-by-side, with transistor gates (red) and dummy gates (orange) regularly spaced apart," and a region delineated by a pink box. *Id*. at 31 (citing Ex. 1002 ¶ 105), 33 (citing Ex. 1011, 12:34–38, 13:57–14:12; Ex. 1002 ¶ 108). According to Petitioner, cells 400 and 500 in Figure 4+5 "are unchanged except that that the top portions of gates 414–418 are slightly extended to provide room for placing gate contacts." *Id*. at 32 n.19. Petitioner contends that "Figure 4+5 combines two adjacent embodiments of Yano in accordance with Yano's teachings and with conventional standard cell layout, and thus would have been obvious to a

POSITA." *Id*. at 32 (citing Ex. 1002 ¶ 106). To support its contention, Petitioner relies on *Boston Scientific Scimed, Inc. v. Cordis Corp.*, in which the court stated that "[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness." *Id*. at 32 n.19 (quoting *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009)); Pet. Reply 5 (same).

Patent Owner argues that Yano's Figure 4 and Figure 5 "illustrate different embodiments, and cannot inherently be combined into a single cell" as depicted in Figure 4+5. PO Resp. 23 (internal citation omitted). Patent Owner argues that Yano's Figure 4 and Figure 5 "are only illustrations of Yano's specific claims, which focus on suppressing variations in manufactured final gate dimensions." *Id*. (citing Ex. 2074 ¶ 138). Patent Owner also argues that "Yano does not expressly disclose any complete semiconductor chip," and that Petitioner "circumvent[s] these contrary teachings in Yano" by combining and altering two different embodiments of Yano "to try to create a layout where all gates in the arbitrary region . . . have the same gate length (which is contrary to every embodiment in Yano)." *Id*. at 16–17.

In an obviousness analysis, a sufficient reason must be shown as to why a POSITA would have thought of combining or modifying the prior art to achieve the patented invention. *See Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008). We have considered the arguments and evidence of record, and determine that Petitioner does not sufficiently establish that a POSITA would have combined and modified the different embodiments depicted in Yano's Figure 4 and Figure 5 to create Figure 4+5 in the manner proposed by Petitioner. In particular, we are not persuaded that Petitioner's reliance on *Boston Scientific* overcomes its lack of

explanation as to why a POSITA would have combined the different embodiments depicted in Figure 4 and Figure 5. It is not sufficient to demonstrate that each of the components in a challenged claim is known in the prior art; Petitioner must also explain why a POSITA would have combined the elements disclosed in the separate embodiments described in Yano. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007) ("a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art"). That the elements are disclosed in separate embodiments of the same reference does not excuse this requirement. *See In re Stepan*, 868 F.3d 1342, 1345–46 n.1 (Fed. Cir. 2017) ("Whether a rejection is based on combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.").

The court in *Boston Scientific* articulated a rationale for why a POSITA would have been motivated to combine two embodiments of a prior art patent in the manner recited in the challenged claims. *Boston Scientific*, 554 F.3d at 991. In *Boston Scientific*, a first embodiment showed a drug-eluting polymer stent made of a drug-eluting polymer with a barrier topcoat (referred to as separate layers), and a second embodiment showed a metallic stent with a drug-eluting polymer coating that was identified with the same numeral as the drug-eluting polymer in the first embodiment. *Id*. at 988. The court found that the motivation to add the second coating layer from the first embodiment to the stent in the second embodiment was the expectation

of achieving the same benefit realized by the use of the second coating layer in the stent in the first embodiment. *Id*. at 991.

Here, Petitioner does not cite any authority supporting the proposition that the adjacent placement of embodiments in a prior art reference, by itself, is a sufficient rationale for combining these embodiments. The court's analysis in *Boston Scientific* indicates that adjacent placement alone is not sufficient. Accordingly, the fact that Yano describes the fifth embodiment shown in Figure 5 immediately after discussing the fourth embodiment shown in Figure 4 is not by itself sufficient to show a reason or motivation to combine the features of those embodiments in the manner set forth by Petitioner.

Petitioner also contends that all of the embodiments in Yano are from the same standard cell library, and, therefore, combining standard cells 400 and 500 as proposed in Figure 4+5 is consistent with conventional standard cell layout. Pet. 30–33; Pet. Reply 5–8. To support its contention, Petitioner points to Yano's statement that "[t]he present invention relates to a standard cell used in a semiconductor integrated circuit, a standard cell library, and a semiconductor integrated circuit using it." Pet. 30 (quoting Ex. 1011, 1:16–19); Pet. Reply 7 (same). As we understand it, Petitioner is arguing that because Yano states that its invention relates to a semiconductor integrated circuit using a standard cell library that includes a standard cell, all of the standard cells disclosed in Yano belong to the same standard cell library.

Petitioner's argument does not account for Yano's other statements regarding standard cell libraries and semiconductor integrated circuits. In particular, after summarizing each of its first through sixth embodiments (including the fourth embodiment, Figure 4, and the fifth embodiment, Figure 5), Yano goes on to state:

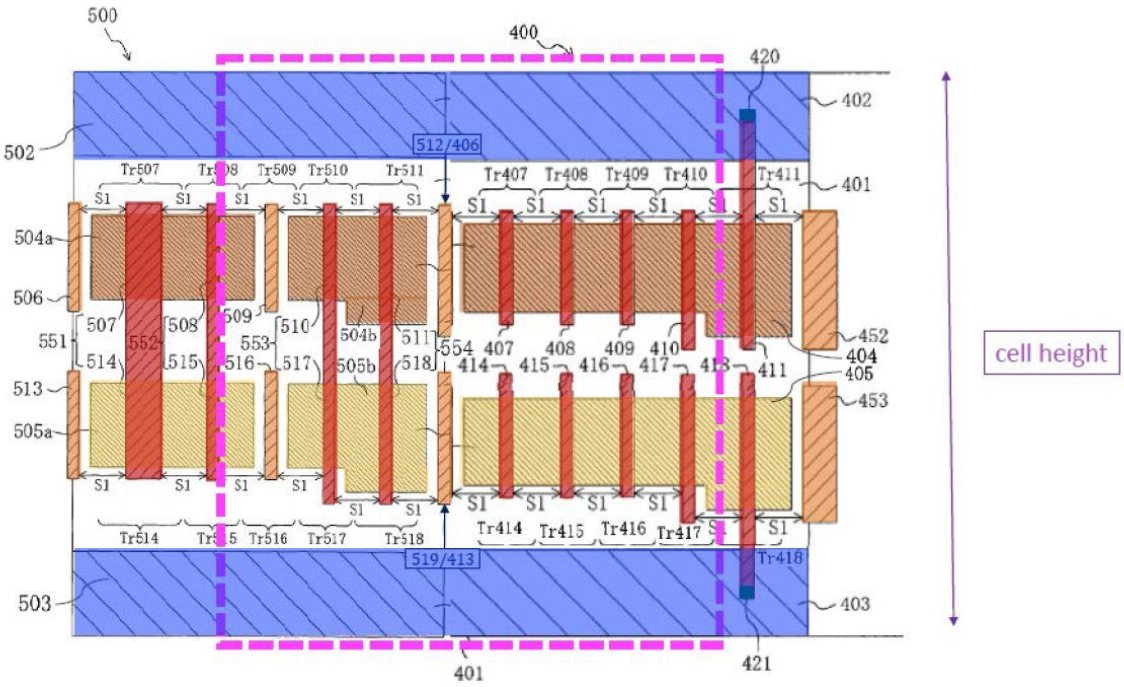
> In a standard cell library *including at least one standard cell according to any one of the first to sixth invention*, variation in characteristics is suppressed.
>
> In a semiconductor integrated circuit *including at least one standard cell according to any one of the first to sixth invention*, variation in characteristics is suppressed.

Ex. 1011, 6:62–67 (emphasis added). We are directed to no statements in Yano that indicate that embodiments one through six are *necessarily* in the same standard cell library or can be used in the same semiconductor integrated circuit. Yano also states that "[i]t is should be noted that only the standard cells are described in the first to sixth embodiments but it is needless to say that the same effects can be obtained in standard cell libraries and semiconductor integrated circuits which include such standard cells." *Id*. at 16:8–12. Notably, Yano does not expressly state that any of the standard cells described in Yano's first through sixth embodiments are part of the same standard cell library, as Petitioner's counsel acknowledged at the hearing. *See* Tr. 18:7–18 (Petitioner's counsel stating that there is not "an express statement in Yano that says cells 400 and 500 are part of the same standard cell library").

Accordingly, we are not persuaded by Petitioner's argument that Yano's statement that "[t]he present invention relates to a standard cell used in a semiconductor integrated circuit, a standard cell library, and a semiconductor integrated circuit using it" establishes that the standard cells described in Yano necessarily belong to the same standard cell library. Instead, it is merely a general characterization of Yano's invention, and does not say anything about the details of the invention.

Petitioner further argues that Yano teaches combining standard cells "of which height, source wiring structure, and the like are uniformed."

Pet. Reply 7 (citing Ex. 1011, 1:16–23, 7:1–12; Ex. 2097, 258:1–18). Petitioner contends that the annotated version of Figure 4+5 ("Annotated Figure 4+5"), reproduced below, "shows that cells 400 and 500 have the same height and share source wirings (blue)." *Id*. at 7–8 (citing Ex. 1062 ¶ 29).



Yano Figure 4+5

Annotated Figure 4+5 shows Yano's standard cells 400 and 500 laid out side-by-side, with transistor gates in red, dummy gates in orange, source wirings in blue, a region delineated by a pink box, and a purple arrowed line added on the right-hand side labeled "cell height." Pet. 31–33; Pet. Reply 7–8. Dr. Shanfield testifies that Annotated Figure 4+5 is consistent with Yano's teaching that cells of uniform height can be combined. Ex. 1062 ¶ 29. With regard to the creation of Annotated Figure 4+5, Dr. Shanfield testifies that

> [a]ll I did was take figure 4 and figure 5 and do what Yano said, which is make the height and source wiring structure uniform. So it was clear that what was being referred to, even though these drawings weren't necessarily perfect—of perfect scale, that you make the source wiring structure and you make the height uniform.

Ex. 2120, 122:12–19.

Patent Owner argues that Yano's Figure 4 and Figure 5 "are disclosed at different scales" and "do not have uniformed height." PO Sur-Reply 12. In that regard, Dr. Khatri testifies that he measured the cells depicted in Yano's Figure 4 and Figure 5, then compared: (1) the ratio of the height of cell 500 to cell 400 to the ratio of the dimensions S1 in cell 500 and 400, and (2) the ratio of the minimum widths of the "thinner gates in Figure 5" to the ratio "with the widths of the thinner gates of Figure 4." Ex. 1061, 93:16–94:5, 95:6–18. Dr. Khatri further testifies that:

> I've found that the ratio of the cell height does not match the ratio of the spacings S1 between the two cells, as well as the ratio of the thin gates in Figures 5 and 4.
>
> So a person of skill in the art would realize that if they were going to try to match the heights of cell [500] and [400], then the gate widths would not match or the gate spacings won't match. If they try to match the spacings, the heights won't match.
>
> And, therefore, they would be much stronger in their conclusion or their determination . . . that cell 500 in Figure 5 and cell 400 and 450 in Figure 4 are from different cell libraries.

Id. at 95:19–96:12.

Dr. Shanfield and Dr. Khatri each base their opinions on the relative sizes of the cells as depicted in Yano's Figure 4 and Figure 5, without providing any intrinsic evidence that Yano's figures are accurate or drawn to scale. *See Hockerson-Halberstadt, Inc. v. Avia Grp., Int'l, Inc.*, 222 F.3d

951, 956 (Fed. Cir. 2000) ("[P]atent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue."). For example, Yano uses "S1" to label the spacing between the gates in each of its standard cells (Ex. 1011, Figs. 1–5), but is silent as to whether the distance represented by S1 is the same for every cell. *See id.* at 7:54–14:56; *see also id*. at Figs. 8–11 (also depicting prior art cells using "S1" to label the spacing between gates). Yano also describes the relative difference in gate lengths within each of standard cells 400 and 500, but does not provide any information comparing the gate lengths in standard cell 400 to those in standard cell 500. *See, e.g.*, *id*. at 12:58-60 (in standard cell 400, dummy gates 452 and 453 have gate length larger than that of gate 411), 14:14–16 (in standard cell 500, gates 507 and 514 have gate length larger than that of the other gates).

We do not discern, nor are we directed to, any disclosures in Yano regarding the size of any of the standard cells (and the elements therein) relative to any of the other standard cells. Nor does Yano provide any information regarding the scale of the drawings in its figures. Because the proportions of Yano's Figure 4 and Figure 5 are not precisely defined, we are not persuaded that Yano discloses the particular size of either one, or how those sizes relate to each other. *See Hockerson-Halberstadt*, 222 F.3d at 956.

Dr. Shanfield also testifies that combining two cells, such as those depicted in Yano's Figure 4 and Figure 5, is consistent with a typical standard cell chip layout. Ex. 1002 ¶ 106 (citing Ex. 1027, 21–22, Fig. 1.5; Ex. 1025, 274, Fig. 8-7). To the extent that Dr. Shanfield is asserting that a POSITA "could" have combined and modified Yano's standard cells 400 and 500 to reach the claimed invention, this is insufficient to support a

finding of obviousness. *See Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–994 (Fed Cir. 2017) (saying that references could be combined "does not imply a motivation to pick [the references] and combine them to arrive at the claimed inventions."); *see also In re Stepan*, 868 F.3d at 1345–46 n.1. "Obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of the prior art to arrive at the claimed inventions." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

Dr. Shanfield, thus, offers only the general proposition that combining two cells in a standard cell chip layout was consistent with standard cell layout, but this does not provide a reason why a POSITA would have been motivated to combine Yano's standard cell 400 with Yano's standard cell 500 in particular. Ex. 1002 ¶ 106; Ex. 1062 ¶ 30. Dr. Shanfield's testimony with respect to the modification of Yano, and Petitioner's arguments that rely on that testimony, leave an analytical gap that does not apprise us of why a POSITA would have combined Yano's standard cells 400 and 500 in the specific manner proposed by Petitioner to create a cell that has gate electrode features formed within a region of the semiconductor chip as required by the challenged claims of the '523 patent. Petitioner would have had to explain what would have led a POSITA at the time of the invention to consider modifying Yano as proposed. Petitioner failed to provide such an explanation. *See W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553 (Fed. Cir. 1983) (In an obviousness analysis, we must "cast the mind back to the time the invention was made" and "occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art.").

It is Petitioner's burden to establish facts supporting its challenge that claims 1, 2, 8–12, 25, and 26 would have been obvious over the combined teachings of Yano, Kitabayashi, and Ikoma by a preponderance of the evidence. 35 U.S.C. § 316(e); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). "Failure to prove the matter as required by the applicable standards means that the party with the burden of persuasion loses on that point—thus, if the fact trier of the issue is left uncertain, the party with the burden loses." *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008). All of Petitioner's arguments relating to the invalidity of claims 1, 2, 8–12, 25, and 26 are premised on the combination of Yano's standard cells 400 and 500 as depicted in Petitioner's Figure 4+5. *See* Pet. 30–95. For the reasons set forth above, we determine that Petitioner has not sufficiently shown that a POSITA would have combined Yano's standard cells 400 and 500 as depicted in Figure 4+5. Therefore, we are not persuaded that Petitioner has made a sufficient showing that a POSITA would have combined the teachings of Yano, Kitabayashi, and Ikoma in the manner proposed. *See Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-00582, Paper 34 (PTAB Aug. 5, 2019) (informative); *Johns Manville Corp. v. Knauf Insulation, Inc.*, IPR2018-00827, Paper 9 (PTAB Oct. 16, 2018) (informative).

Accordingly, we conclude that Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 8–12, 25, and 26 are

unpatentable under 35 U.S.C. § 103 as obvious over the combined teachings of Yano, Kitabayashi, and Ikoma.[5]

III. PATENT OWNER'S MOTION TO EXCLUDE

Patent Owner moves to exclude Exhibit 1068, Exhibit 1071, and paragraphs 81–83, 90, and 91 of Exhibit 1062. Paper 54. We do not reach the merits of Patent Owner's Motion to Exclude, because our Decision does not rely on Exhibit 1068, Exhibit 1071, and paragraphs 81–83, 90, and 91 of Exhibit 1062.[6] Accordingly, we dismiss Petitioner's Motion to Exclude as moot.

IV. CONCLUSION

For the reasons given, we are not persuaded that Petitioner has shown by a preponderance of the evidence that claims 1, 2, 8–12, 25, and 26 of the '523 patent would have been unpatentable based on the challenge presented in the Petition.

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[5] Patent Owner argues that objective indicia support the nonobviousness of the challenged claims. PO Resp. 59–68. Because we find that Petitioner has not demonstrated that the claims would have been obvious over the asserted prior art, we need not address Patent Owner's evidence of objective indicia. *See Hamilton Beach Brands, Inc. v. f'real Foods, LLC*, 908 F.3d 1328, 1343 (Fed. Cir. 2018) (holding that "objective indicia of nonobviousness" "need not [be] addressed" because the court "affirmed the Board's findings regarding the failure of the prior art to teach or suggest all [claim] limitations").

[6] Exhibit 1068, Exhibit 1071, and paragraphs 81–83, 90, and 91 of Exhibit 1062 are relevant only to Patent Owner's arguments regarding objective indicia of nonobvious, which we do not address in this Decision.

In summary:

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 2, 8–12, 25, 26	103	Yano, Kitabayashi, Ikoma		1, 2, 8–12, 25, 26
Overall Outcome				1, 2, 8–12, 25, 26

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 8–12, 25, and 26 of the '523 patent are unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude (Paper 54) is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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