UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner

v.

QUALCOMM INC.,
Patent Owner.

IPR2018-01460
Patent 9,024,418 B2

Before MICHELLE N. WORMMEESTER, AMANDA F. WIEKER, and AARON W. MOORE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

JUDGMENT
FINAL WRITTEN DECISION
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

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I. INTRODUCTION

A. Background

Apple Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–5, 8–10, and 12–20 of U.S. Patent No. 9,024,418 B2 (Ex. 1001, "the '418 patent"). Paper 2 ("Pet."). Qualcomm Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

On March 15, 2019, we instituted an *inter partes* review of claims 1–5, 8–10, and 12–20. Paper 7 ("Inst. Dec.") 20. Patent Owner then filed a Patent Owner Response (Paper 20, "PO Resp."), Petitioner filed a Reply (Paper 36, "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 39, "PO Sur-Reply").

An oral hearing was held on December 12, 2019, and a transcript of the hearing is included in the record. Papers 46, 47 ("Tr.").

The Board has jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner *has* shown by a preponderance of the evidence that claims 3, 9, 10, and 14 of the '418 patent are unpatentable, and that Petitioner *has not* shown that claims 1, 2, 4, 5, 8, 12, 13, 15–19, and 20 are unpatentable.

B. Related Matters

The '418 patent was at issue in *Qualcomm Incorporated v. Apple Incorporated*, Civil Action No. 3:17-CV-02402 (S.D. Cal.), when the Petition was filed, but that litigation has since been dismissed. *See* Pet. 1; Petitioner's Updated Mandatory Notices (Paper 16) 1.

C. The '418 Patent

The '418 patent concerns "[a] local interconnect structure . . . that includes a gate-directed local interconnect coupled to an adjacent gate layer through a diffusion-directed local interconnect." Ex. 1001, Abstract.

The claimed structure can be explained with reference to Figure 4A, annotated with colors below:

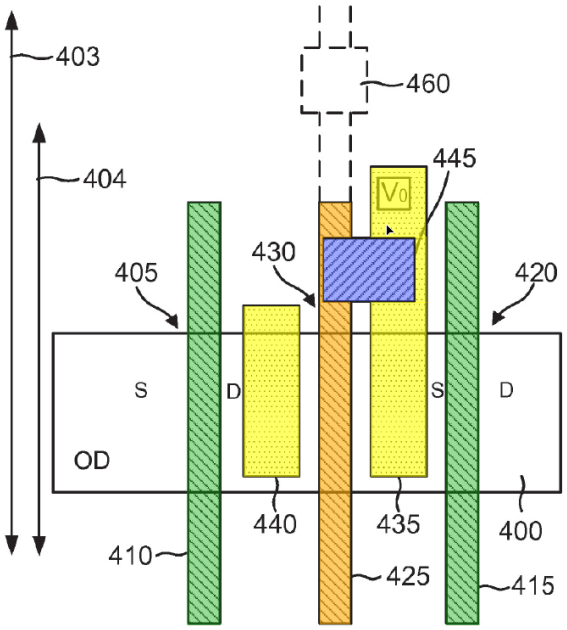

FIG. 4A

Figure 4A shows "the layout for a pair of transistors in a continuous diffusion region including a blocking transistor." Ex. 1001, 3:9–10.

This embodiment[1] includes continuous diffusion layer 400, which forms the basis for two transistors. The transistors consist of gate layers 410 and 415, shown in green, and the associated source and sink regions in the continuous diffusion layer. An additional gate layer 430, shown in orange, operates as a blocking transistor. The source region for the right transistor is

[1] *See* Ex. 1001, 5:66–7:3.

provided with voltage by local interconnect 435, shown in yellow, which is biased by via V_0. Local interconnect 445 couples interconnect 435 and gate layer 430. The gate layers and interconnect 435 are "gate directed," which in this context means that their long dimensions are perpendicular to the length of the continuous diffusion layer; the local interconnect 445 is "diffusion directed," which in this context means that its long dimension is parallel to the length of the continuous diffusion layer.

The '418 patent explains that because "[v]ias require a certain separation between them . . . the square-shaped local interconnect 460 of the prior art"—shown in dashed outline in Fig 4A—"had to be displaced vertically from via V_0 to accommodate the via pitch," and that the '418 patent's "diffusion-directed local interconnect 445 eliminates the need for such a vertically-displaced coupling to gate layer 425" and thus "has an advantageously reduced cell height 404 for transistors 405 and 420 as compared to conventional cell height 403, which enhances density." Ex. 1001, 6:60–7:3.

D. The Claimed Subject Matter

Independent claims 1, 12, and 17, reproduced below, illustrate the subject matter addressed in this proceeding. Claim 1 is directed to a circuit, claim 12 is directed to a method corresponding to the circuit of claim 1, and claim 17 is directed to a similar circuit, but drafted using means-plus-function terminology:

1. A circuit comprising:

   a first gate layer arranged according to a gate layer pitch between a second gate layer and a third gate layer;

a first gate-directed local interconnect arranged between the first gate layer and the second gate layer;

a second gate-directed local interconnect arranged between the first gate layer and the third gate layer; and

a diffusion-directed local interconnect layer configured to couple the first gate layer to one of the first and second gate-directed local interconnects, wherein the first gate-directed local interconnect, the second gate-directed local interconnect, and the diffusion-directed local interconnect are all located between a lower-most metal layer and a semiconductor substrate for the circuit.

12. A method, comprising:

forming a first gate layer over a semiconductor substrate according to a gate layer pitch between adjacent second and third gate layers;

forming a first gate-directed local interconnect between the first gate layer and the second gate layer;

forming a second gate-directed local interconnect between the first gate layer and the third gate layer; and

forming a diffusion-directed local interconnect to couple one of the first and second gate-connected local interconnects to the first gate layer, wherein the first gate-directed local interconnect, the second gate-directed local interconnect, and the diffusion-directed local interconnect are all located between the semiconductor substrate and an adjacent lower-most metal layer.

17. A circuit comprising:

a continuous diffusion region within a semiconductor substrate;

a pair of gate layers configured to form gates for a pair of transistors having source/drain terminals in the continuous diffusion region;

a third gate layer arranged between the pair of gate layers to form a gate for a blocking transistor;

> a gate-directed local interconnect configured to couple to a drain/source terminal for a transistor in the pair of transistors; and
>
> means for coupling the gate-directed local interconnect to the third gate layer, wherein the gate-directed local interconnect and the means are both located between the semiconductor substrate and an adjacent lower-most metal layer.

Ex. 1001, 9:6–19, 10:5–18, 10:38–52.

E. Evidence Relied Upon

Petitioner relies on the following references:

Reference		Exhibit
Rashed	US 8,618,607 B2	1005
Lu	US 9,123,565 B2	1006
Nauta	Bram Nauta, A CMOS Transconductance-C Filter Technique For Very High Frequencies, *IEEE Journal of Solid-State Circuits*, Vol. 27, Issue 2 (Feb 1992)	1007

Petitioner also relies on a Declaration of David Kuan-Yu Liu, filed as Exhibit 1003 ("Liu Decl."). Patent Owner relies on a Declaration of Dr. Pradeep Lall, filed as Exhibit 2002 ("Lall Decl.").

1. Rashed

Rashed describes "semiconductor devices formed in and above a continuous active region and a conductive isolating structure formed above the active region between the devices." Ex. 1005, 1:13–15.

One example is shown in Figure 4A, which is reproduced below. As shown, the source regions of adjacent transistors are coupled to power rail 140H by conductive structures 144 (in yellow). *See* Ex. 1001, 6:21–36.

Isolating electrode 150PG (in orange) is positioned between adjacent source regions of the continuous active region, and is also connected to the power rail. *See id*., 5:17–20, 6:21–36. Gate structures 130 (in green) are formed across the active region between the source regions and corresponding drain regions. *See id*. 4:60–66.

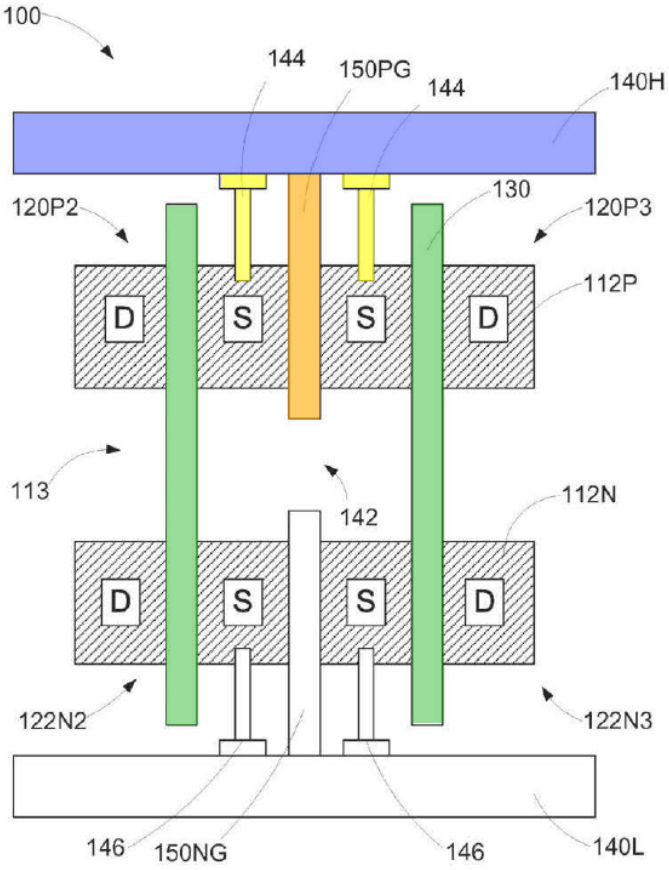

Figure 4A

Figure 4A of Rashed is a schematic depiction of an exemplary semiconductor device. See Ex. 1001, 3:29–31.

2. Nauta

Nauta is an article describing "CMOS circuits for integrated analog filters at very high frequencies." Ex. 1007, Abstract. In pertinent part, it describes a common-mode voltage inverter circuit, shown in Fig. 2(b), in which the gates of both the PFET and NFET of the inverter are tied to the drains of both the PFET and NFET. *See* Ex. 1003 (Liu Decl.) pp. 56–58.

F. Grounds of Unpatentability

This trial was instituted on the following grounds:

Reference(s)	35 U.S.C. §	Claim(s) Challenged
Rashed	102	1–3, 5, 8, 9, 12–14, 16–19
Rashed	103	1–3, 5, 8, 9, 12–14, 16–19
Rashed, Lu	103	4, 15, 20
Rashed, Nauta	103	10

II. ANALYSIS

We discuss below the level of skill in the art, claim construction, antedating Rashed and Lu, the patentability of the present claims.

A. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art "would have had a Master's of Science Degree (or a similar technical Master's Degree, or higher degree) in an academic area emphasizing electrical engineering or computer engineering with a concentration in semiconductors or, alternatively, a Bachelors Degree (or higher degree) in an academic area emphasizing electrical or computer engineering and having two or more years of experience in integrated circuit design and/or semiconductor

processing." Pet. 10–11. Petitioner adds that "[a]dditional education in a relevant field, such as computer engineering, or electrical engineering, or industry experience may compensate for a deficit in one of the other aspects of the requirements stated above." *Id*. at 11.

Patent Owner asserts that a person of ordinary skill in the art "would have had (a) a Bachelor's of science degree in an engineering discipline or physics, or a closely-related field, and at least two years of work or research experience in the field of semiconductor design or fabrication, or (b) a Master's of science degree in an engineering discipline or physics, or a closely related field, and at least one year of work or research experience in that same field." PO Resp. 5 (citing Ex. 2002 ¶¶ 33–36).

Although the parties do not agree on the correct formulation, neither argues why theirs is superior or that the selection of one or the other makes a difference in the outcome of this case. Under these circumstances, we adopt Petitioner's characterization of the level of ordinary skill in the art, which we find to be generally consistent with the disclosures of the patent and the cited prior art.

B. Claim Construction

In *inter partes* reviews filed before November 13, 2018, such as this one, claims of an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b) (2017); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016); 83 Fed. Reg. 51,340. Under that standard, claim terms are generally given their ordinary and customary meaning, as would have been understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc*.,

504 F.3d 1249, 1257 (Fed. Cir. 2007). We address below the terms that at least one party identified as requiring construction.

1. "means for coupling the gate-directed local interconnect to the third gate layer"

Claim 17 recites "means for coupling the gate-directed local interconnect to the third gate layer, wherein the gate-directed local interconnect and the means are both located between the semiconductor substrate and an adjacent lower-most metal layer." The Petition argued that "[t]he 'means' in 'means for coupling' encompasses a 'diffusion-directed local interconnect.'" Pet. 13 (citing Ex. 1001, 5:62–64, 6:36–38, 7:9–12; Figs. 4A, 4B, 5A, 5B).

Patent Owner asserts that "[i]n the co-pending litigation, Petitioner agreed to a proper identification of corresponding structure as: 'a diffusion-directed local interconnect as described at 7:8–12, Fig. 4A, 3:9–14, Fig. 4B, 3:15–19, 7:12–16, 5:62–64, 6:36–39, 8:9–11, 2:48–52, Figs. 5A, 5B, 6A, 7A, or 7B, and equivalents thereof.'" PO Resp. 6 (citing Ex. 2001, 26–28). Patent Owner argues that "[f]or each corresponding structure, the diffusion-directed local interconnect—and the diffusion-directed local interconnect alone—performs the claimed function" and that "[n]one of the diffusion-directed local interconnects rely upon other structures, for example an intermediate connection, to complete the physical connection between the gate-directed local interconnect or gate layer." *Id*. at 6–7 (citing Ex. 1002 ¶ 42).

Petitioner's Reply does not address this issue, and we agree with Patent Owner that the corresponding structure is a diffusion-directed local interconnect as described in the '418 patent at 7:8–12, 3:9–14, 3:15–19,

7:12–16, 5:62–64, 6:36–39, 8:9–11, 2:48–52 and shown in Figs. 4A, 4B, 5A, 5B, 6A, 7A, and 7B, as well as equivalents thereof. We note that neither party has addressed the scope of the "equivalents thereof."

2. "configured to" and "forming . . . to"

Patent Owner argues that "the phrase 'configured to' in claim 1 should be construed as 'requiring structure designed to or configured to accomplish the specified objective, not simply that they can be made to serve that purpose.'" PO Resp. 7. According to Patent Owner, the Federal Circuit has explained that "configured to" requires that the claimed structures "are designed or configured to accomplish the specified objective, not simply that they can be made to serve that purpose." PO Resp. 8 (citing *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1349 (Fed. Cir. 2012)). Patent Owner further argues that, for similar reasons, "the 'forming . . . to' language of Claim 12 should be given the same interpretation." *Id*.

Petitioner does not address this issue, and we agree with Patent Owner that, on this record, "configured to" and "formed to" mean that the structure is designed or constructed to accomplish the specified objective. *Cf. In re Giannelli*, 739 F.3d 1375, 1379 (Fed. Cir. 2014) (distinguishing between "configured to" and "capable of" or "suitable for"). As explained below, however, we do not agree with Patent Owner that this interpretation distinguishes the claims over Rashed.

3. "diffusion-directed local interconnect"

Patent Owner contends that "[i]n the litigation, Patent Owner and Petitioner agreed that ['diffusion-directed local interconnect'] means: 'a local interconnect that has a polygonal footprint with a longitudinal axis that

is parallel to the longitudinal axes of the polygonal footprints of the diffusion regions.'" PO Resp. 10 (citing Ex. 2001, 21, 31).

Petitioner does not respond to Patent Owner's argument, and, finding Patent Owner's proposed construction consistent with the definition in the Specification (*see* Ex. 1001, 4:39–43), we adopt it.

4. "first gate layer for the second transistor to a power supply node"

Patent Owner argues that claim 5 "includes an obvious typographical error in the phrase 'first gate layer for the second transistor' and would be readily understood by a POSITA as 'first gate layer for the blocking transistor.'" PO Resp. 10 (citing Ex. 2002 ¶ 43). Patent Owner asserts that claim 2, "from which claim 5 depends, provides antecedent basis for claim 5 and states that 'the first gate layer comprises a gate for a blocking transistor' and "also recites an 'adjacent second transistor,' that is therefore not the same as the 'blocking transistor.'" *Id*. Petitioner responds that "a Patent Owner Response is not the proper vehicle for such a corrective amendment," which should instead be pursued in a Motion to Amend. Pet. Reply 26.

Given that the parties both acknowledge the claim is defective as written,[2] that Patent Owner's proposed "construction" reflects a change more appropriately pursued by other means, such as a certificate of correction or motion to amend, and that neither party offers thorough analysis or argument as to how or why this claim should, or should not, be

[2] *See, e.g.,* Pet. 39–40 ("[T]he phrase 'first gate layer for the second transistor,' in claim 5 is inconsistent with claim 2, and therefore should not be given patentable weight."); PO Resp. 10 (acknowledging the "obvious typographical error").

construed as Patent Owner proposes, we conclude that we are not able to construe claim 5 on this record. We further determine that "the proper course for [us] to follow" under these circumstances is to "conclude that [we cannot] reach a decision on the merits with respect to whether petitioner had established the unpatentability" of claim 5. *Samsung Elecs. Am., Inc. v. Prisua Engr. Corp.*, 948 F.3d 1342, 1353 (Fed. Cir. 2020); *see In re Steele*, 305 F.2d 859, 862 (Cust. & Pat. App. 1962) (explaining that prior art rejections should not be based on "speculation as to meaning of the terms employed and assumptions as to the scope of such claims"). Petitioner, therefore, has not met its burden to demonstrate, by a preponderance of the evidence, that claim 5 unpatentable.

C. Antedating Rashed and Lu

Patent Owner argues that "[t]he inventors' invention of [claims 1, 2, 4, 5, 8, 12, 13, 15–18, and 20] antedates both Rashed and Lu." PO Resp. 11.[3] In particular, Patent Owner argues that the inventors conceived of the subject matter of these claims "no later than January 17, 2012" and that they "were reduced to practice no later than June 28, 2012 through fabrication and testing of a test chip embodying the [claimed subject matter]." *Id*.

1. Sufficiency of Patent Owner's Conception Evidence

An inventor can swear behind a reference by proving conception of the invention before the effective filing date of the reference and diligent

[3] Patent Owner does not seek to antedate challenged claims 3, 9, 10, 14, and 19, and we consider patentability of those claims in light of Rashed and Lu in Section II.D. Due to the claim construction problem, we do not consider whether claim 5 can antedate the references.

reduction of the invention to practice after that date. *See Apator Miitors ApS v. Kamstrup A/S*, 887 F.3d 1293, 1295 (Fed. Cir. 2018) (citing *Perfect Surgical Techniques, Inc. v. Olympus Am., Inc.*, 841 F.3d 1004, 1007 (Fed. Cir. 2016)). "[W]hen a party seeks to prove conception through an inventor's testimony," however, "the party must proffer evidence, 'in addition to [the inventor's] own statements and documents,' corroborating the inventor's testimony." *Apator Miitors*, 887 F.3d at 1295 (quoting *Mahurkar v. C.R. Bard, Inc.*, 79 F.3d 1572, 1577 (Fed. Cir. 1996)).

Patent Owner offers testimony by "[i]nventors Giridhar Nallapati and John Zhu . . . that by January 17, 2012, the inventors had a definite and permanent idea of the complete and operative invention disclosed in the '418 Patent." PO Resp. 12 (citing Ex. 2060 (Nallapati Declaration) ¶¶ 2–3; Ex. 2061 (Zhu Declaration) ¶¶ 2–3).

Patent Owner further argues that the inventor testimony "is corroborated by a January 17, 2012 GDS file," named "qptc20_1t_top_fill_no215_20120117.gds.gz," corresponding to "a test chip known as QPTC20_1T, which contains a test device known as 'Device Under Test 16' ('DUT 16') embodying the invention disclosed in the '418 Patent." PO Resp. 12 (citing Ex. 2060 ¶¶ 4, 77–107; Ex. 2061 ¶¶ 4, 41–71; Ex. 2002 (Lall Decl.) ¶¶ 44–67). Patent Owner contends that "DUT 16 contains multiple repetitions of structures known internally as 'MP over OD' or 'Continuous OD'" and that "DUT 16 embodies all elements" of the subject claims. PO Resp. 12.

According to Patent Owner, "[t]he date of the GDS file 'qptc20_1t_top_fill_no215_20120117.gds.gz' is verified in four ways": (1) "multiple declarants testify that the file name itself—here '20120117'—

indicates the finalization date of the file based on Qualcomm's naming convention practice," (2) "page 1 of [Ex. 2005] and page 1 of [Ex. 2006] are screenshots that show the Qualcomm file server where the file is stored showing the last modified date as 9 am January 18, 2012," (3) Ex. 2010 "is a contemporaneous e-mail from the project lead Dr. Frank (Bin) Yang stating 'the final version QTC20_1T taped out to TSMC has been completed on Tuesday, Jan. 17th 2012,' which Dr. Yang testifies is accurate and refers to [the] GDS file," and (4) Ex. 2007 is "screenshots showing submission of the same file through Qualcomm's Tapeout Manager Program with a date stamp of January 17, 2012." PO Resp. 12–13 (citing Ex. 2060 ¶¶ 7, 112; Ex. 2061, ¶¶ 7, 76; Ex. 2062, ¶¶ 7–9, 58–62; Ex. 2010, 1–2; Ex. 2007, 1, 8).

Petitioner argues that Patent Owner "relies on uncorroborated testimony from the inventors of the '418 patent . . . to support its allegation that the [claimed subject matter was] conceived prior to the effective dates of Rashed and Lu," that "such uncorroborated inventor testimony is insufficient to show conception," and that "thus [Patent Owner]'s argument fails." Pet. Reply 6.

Petitioner also argues that Patent Owner "fails to identify any evidence to corroborate that Nallapati and Zhu alone were, in fact, the individuals that conceived of the alleged invention." *Id*. at 7 (emphasis omitted). Petitioner contends that Patent Owner "does not allege that any information in the 'January 17, 2012 GDS file,' or any other evidence of record in the present proceeding, shows that Nallapati and Zhu were the individuals that conceived of the subject matter in the January 17, 2012 GDS file." *Id*. at 8 (emphasis omitted).

Petitioner further argues that "[t]he screenshots in Ex. 2006, which were created by Dr. Zhu, are uncorroborated inventor testimony, and are thus insufficient to support a showing of conception." Pet. Reply 9. Petitioner argues that "[b]y selecting which layers were visible and invisible [in the screenshots], Dr. Zhu effectively provides testimony directing viewers to key features from the GDS file" and "[t]hus, the screenshots in Ex. 2006, which were created by Dr. Zhu, an inventor, specifically for the purposes of Qualcomm's swear-behind argument, should be treated as inventor testimony." *Id*. at 10.

We are not persuaded by Petitioner's arguments. The "rule of reason" analysis applied to corroboration "requires an evaluation of all pertinent evidence when determining the credibility of an inventor's testimony" and, notably, "it is not necessary to produce an actual over-the-shoulder observer" and "sufficient circumstantial evidence of an independent nature can satisfy the corroboration requirement." *Cooper v. Goldfarb*, 154 F.3d 1321, 1330 (Fed. Cir. 1998).

We find that the testimony of the two inventors is not "uncorroborated" because (a) the file provides corroboration of the testimony, (b) the file is dated and the date is corroborated in multiple ways, (c) the inventors' testimony is confirmed by Dr. Yang, who is not an inventor, and the screenshots from the tapeout system, and (d) the testimony and documents are further verified Dr. Ranganathan, who also is not an inventor.

It is true, as Patent Owner observes, that we have only the testimony of the inventors that it was they who actually conceived of the inventive structures, but such is frequently the case. The law does not require

independent, conclusive proof that the inventor is the one who had the mental spark of invention; rather, what is needed is "only that the corroborative evidence, including circumstantial evidence, support the credibility of the inventors' story." *E.I. du Pont De Nemours & Co. v. Unifrax I LLC*, 921 F.3d 1060, 1077 (Fed. Cir. 2019) (citing *NFC Tech., LLC v. Matal*, 871 F.3d 1367, 1371 (Fed. Cir. 2017)). The cases do not require "that evidence have a source independent of the inventors on every aspect of conception and reduction to practice" as "such a standard [would be] the antithesis of the rule of reason." *E.I. du Pont De Nemours*, 921 F.3d at 1077 (quoting *Cooper*, 154 F.3d at 1331); *see NFC Tech.*, 871 F.3d at 1372 ("[A]n inventor's conception can be corroborated even though 'no one piece of evidence in and of itself' establishes that fact," and "even through circumstantial evidence," because "[a]t bottom, the goal of the analysis is to determine 'whether the inventor's story is credible.'") (citations omitted).

We find that the evidence offered by Patent Owner, as described above and in the declarations of non-inventors Yang and Ranganathan, is sufficient to support the inventor's story of conception when viewed as a whole, and through the rule of reason lens.

We also do not agree with Petitioner that the screenshots are "inventor testimony." The screenshots are simply views of the large, complex GDS file that remove extraneous structures so that those corresponding to the claims can be viewed clearly. We see no practical difference between inventor Zhu removing irrelevant elements from the view of the file and an inventor directing one to a specific notebook, page, or other material. The evidence is the rendering showing the presence of the relevant structures in the file, which is not testimony. We also note that Petitioner received a copy

of the file, without any extraneous structures having been removed, and also had the opportunity to depose Mr. Zhu and reveal any errors in turning the GDS file into more accessible screenshots. *See* Tr. 40:6–7.

As we are not persuaded by Petitioner's argument that Patent Owner relies only on uncorroborated inventor testimony, we turn to whether the evidence reflects invention of the subject matter of claims 1, 2, 4, 8, 12, 13, 15–18, and 20.

2. Conceived Subject Matter

Patent Owner explains that Ex. 2006 "contains screenshots taken by inventor Zhu of portions of 'qptc20_1t_top_fill_no215_20120117.gds.gz' viewed in a GDS viewer" and that Ex. 2016B "contains images taken with a Transmission Electron Microscope ('TEM') showing cross-sections of the DUT 16 structure as fabricated in accordance with the GDS file." PO Resp. 13–14 (citing Ex. 2061 ¶ 7; Ex. 2063 ¶ 8). According to Patent Owner, "as illustrated by [Ex. 2006] and [Ex. 2016B], the DUT 16 structure as specified in the January 17, 2012 GDS file for QPTC20_1T embodies all [of the subject] claims." *Id*. at 14. The Patent Owner Response details how the structures in DUT 16 meet the limitations of claims 1, 2, 4, 8, 12, 13, 15–18, and 20. *See* PO Resp. 13–32; *see also* Ex. 2006 (GDS screenshots); Ex. 2016B (TEM images); Ex. 2002 (Lall Decl.) ¶¶ 44–67; Ex. 2060 (Nallapati Declaration) ¶¶ 74–108; Ex. 2061 (Zhu Declaration) ¶¶ 38–72. We have reviewed and are persuaded by that analysis with respect to claims 1, 2, 4, 8, 12, 13, 15–18, and 20, which Petitioner does not dispute.

Petitioner *does* dispute the analysis for claims 5 and 16, arguing that although Patent Owner "alleges that metal layer 2 is one of the layers that extends into the Vdd / Ground regions shown in teal on the far right on the

view above," Petitioner's "investigation of the January 17, 2012 GDS file reveals that this is not the case, and that metal layer 2 in fact does not contact these Vdd / Ground regions." Pet. Reply 17. However, due to the claim construction problem, Petitioner is not able to prove claim 5 unpatentable (*see* Section II.B.4) and, as Patent Owner observes, "[c]laim 16 does not recite a 'power supply node,'[4] and thus Petitioner's argument is applicable, at best, to [c]laim 5." PO Sur-Reply 10.

We conclude that Patent Owner has proven, by a preponderance of evidence, conception of the subject matter of claims 1, 2, 4, 8, 12, 13, 15–18, and 20 prior to the effective dates of Rashed and Lu.

3. Reduction to Practice

To establish an actual reduction to practice, an inventor must prove that he or she (1) constructed an embodiment or performed a process that meets all the claimed limitations of the invention, and (2) determined that the invention worked for its intended purpose. *Cooper v. Goldfarb*, 154 F.3d 1321, 1327 (Fed. Cir. 1998).

Patent Owner argues that the subject matter of claims 1, 2, 4, 8, 12, 13, 15–18, and 20 was "reduced to practice by June 28, 2012, which is sufficient to antedate Rashed's July 2, 2012 filing date [and] Lu's February 27, 2013 filing date." PO Resp. 34.

Specifically, Patent Owner argues that "[b]eginning in February 2012, multiple lots of QPTC20_1T6 test chips were fabricated." PO Resp. 34 (citing Ex. 2060 ¶ 189; Ex. 2061 ¶¶ 96–97; Ex. 2062 ¶¶ 78–79; Ex. 2028B).

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[4] Claim 16 recites: "The method of claim 12, further comprising forming a via coupled between the one of the first and second gate directed local interconnects and a first metal layer."

Patent Owner explains that "[e]ach lot of test chips was fabricated in phases, first fabricating layers from the silicon up to the M1 Metal Layer followed by wafer acceptance testing ('WAT'), then continuing to fabricate additional layers." *Id*. at 34–45 (citing Ex. 2060 ¶ 189; Ex. 2061 ¶¶ 96–97; Ex. 2062, ¶¶ 78–79; Ex. 2028B; Ex. 2060 ¶ 156; Ex. 2062 ¶ 81).

According to Patent Owner, "[c]onsistent with the very purpose of GDS files and TSMC's role as a foundry fabricating chips in accordance with the provided GDS file, each test chip contained the test structures defined in "qptc20_1t_top_fill_no215_20120117.gds.gz." PO Resp. 35 (citing Ex. 2060 ¶¶ 72, 146; Ex. 2061 ¶¶ 36, 109; Ex. 2062 ¶¶ 57, 90). This is confirmed, according to Patent Owner, by "Transmission Electron Microscope (TEM) images . . . show[ing] the structures of DUT 16 defined in the GDS file . . . are found in the physical chips." PO Resp. 35 (citing Ex. 2002 ¶¶ 44–67; Ex. 2063 ¶¶ 27–56).

Patent Owner continues that "[a]s of June 28, 2012, the '1st Lot' had been fabricated to include all layers up to the M6 Metal Layer, as indicated by the notation '1P6M' in a June 28, 2012 TSMC status report" and that "[t]hus, by June 28, 2012, the '1st Lot' of QPTC20_1T fabricated through the M6 Metal Layer constituted a physical embodiment of all elements of the subject claims." PO Resp. 35 (citing Ex. 2018, 2; Ex. 2060 ¶¶ 144–145; Ex. 2061 ¶¶ 107–108; Ex. 2062 ¶ 81).

Patent Owner further argues that "QPTC20_1T M1 WAT testing for the '1st Lot,' which was completed and reported to the Qualcomm team by May 24, 2012, demonstrated that the MP over OD concept embodied in the [subject claims] would work for its intended purpose as interconnect

structures for an integrated circuit." PO Resp. 36 (citing Ex. 2060 ¶¶ 139–143; Ex. 2061 ¶¶ 103–106; Ex. 2062 ¶¶ 87–89; Ex. 2015).

Patent Owner explains that "[p]rior to fabrication, a particular focus of the inventors in evaluating whether the MP over OD design would function properly was assessing potential leakage current issues, that testing showed no increased leakage current, and that "[b]ased on the results of this testing, Drs. Nallapati and Zhu testify that they and the Qualcomm team were able to conclude that leakage current was not an issue for the MP over OD design." PO Resp. 36–37 (citing Ex. 2060 ¶¶ 119–120, 135, 142–43; Ex. 2061 ¶¶ 83–84, 99, 105–106; Ex. 2062 ¶¶ 65–66, 89; Ex. 2014C; Ex. 2015).

Petitioner argues that Patent Owner "does not allege that the inventors designed or implemented the structures included in the January 17, 2012 GDS file." Pet. Reply 12. In fact, however, the inventors both testified that their invention was incorporated into the GDS file. *See* Ex. 2060 ¶ 2–4; Ex. 2061 ¶ 2–4.[5]

Petitioner also argues that Patent Owner "provides no information regarding the inventor's involvement in creating [the] GDS file," and that Patent Owner "thus has not shown that the June 28, 2012 test chip, which was allegedly fabricated based on this GDS file, was created by or on behalf of the inventors." Pet. Reply 12. Petitioner similarly argues that

[5] *See, e.g.*, Ex. 2060 ¶ 2 ("I and the other inventors on the '418 Patent conceived of our invention between August 2011 and January 2012 while overcoming 20 nanometer technology challenges to boost performance and area scaling and subsequently developing test structures in the said 20 nanometer semiconductor node. The invention described in the '418 patent was incorporated into several test structures for a Computer Aided Design (CAD) Graphic Database System 'GDS' file that was finalized on or about January 17, 2012.").

"[t]estimony by Dr. Nallapati in his declaration and during his deposition" indicates that others "participated in the design of the January 17, 2012 GDS file." Pet. Reply 12 (citing Ex. 2060 ¶¶ 109, 121; Ex. 2061 ¶ 74; Ex. 1016, 27:11–28:16, 135:20–138:7; Ex. 2007; Ex. 2058).

We are not persuaded by these arguments because we see no reason why the inventors would have needed to create the GDS file themselves. It is sufficient for inventorship that they conceived of the claimed structures that were then reduced to practice. That others (e.g., Mr. Gan, Mr. Bucki, and Dr. Yang) were involved in the creation of the GDS file and its submission to the foundry does not negate inventorship. *See, e.g., Trovan, Ltd. v. Sokymat SA, Irori*, 299 F.3d 1292, 1306 (Fed. Cir. 2002) ("Using the services of other Sokymat employees to bond the wire leads to the gold bumps does not change the fact that Gustafson . . . was the first to reduce the invention to practice."); *Shatterproof Glass Corp. v. Libbey-Owens Ford Co.*, 758 F.2d 613, 624 (Fed. Cir. 1985) ("An inventor may use the services, ideas, and aid of others in the process of perfecting his invention without losing his right to a patent.") (quoting *Hobbs v. United States Atomic Energy Comm'n*, 451 F.2d 849, 864 (5th Cir. 1971)).

Petitioner also argues that "Dr. Nallapati was repeatedly asked during his deposition about whether he and the other inventors designed or implemented the structures in the January 17, 2012 GDS file" and that he "refus[ed] to provide any additional details regarding the design process of the January 17, 2012 GDS file." Pet. Reply 13 (citing Ex. 1017, 139:1–144:8). We do not agree. In the cited portion of the transcript, the witness is asked to identify "evidence" that he and the other inventors invented the claimed structures, and the witnesses responded that the declaration

"provide[s] evidence that the invention was, indeed, incorporated into the standard cell that is used in the ring oscillator circuit." Ex. 1017, 141:6–9. The witness was correct that the evidence of the invention is the inventor testimony, which is corroborated, as explained above. The cited testimony does not reflect a refusal to provide "additional details regarding the design process," as Petitioner argues, because the questioning was not seeking "details regarding the design process."

Petitioner additionally argues that Patent Owner has not shown that the invention would have worked for its intended purpose because Patent Owner "does not provide any evidence that preventing or minimizing 'leakage current' was the intended purpose of the" subject claims. Pet. Reply 14–15.

This is also unpersuasive. The invention was intended to reduce the size of the footprint which, by its very structure, it did. The question for the inventors, then, was whether the reduced footprint design could be used in an actual chip (i.e., would the chip have worked), and the specific concern the inventors had in that regard was that "the 20 nanometer processes might not support the MP structures in close proximity to MD2 structures on the opposite side of the gate layer . . . and there would be undesired leakage current through the unconnected MD2." Ex. 2060 ¶ 119. Inventor Nallapati testified that the results from the testing performed by the foundry confirmed that "the leakage current concerns . . . for the MP over OD structures were not actually an issue" and that "the MP over OD structures . . . worked for their intended purpose." *Id*. at ¶ 135.

Preventing or minimizing leakage current need not have been "the intended purpose of the subject claims," as Petitioner argues. Instead, the

question was whether the structure for achieving the purpose stated in the patent—increasing the density in a continuous OD layout[6]—would have worked in an actual chip. *See Cooper*, 154 F.3d at 1327 ("When testing is necessary, the embodiment relied upon as evidence of priority must actually work for its intended purpose."). The evidence shows that the inventors, having concluded that leakage current was not a problem, determined that the invention would have worked for its intended purpose of increasing density in a working chip.

4. Word Limit

Petitioner also argues that "Qualcomm submits upwards of sixty exhibits with its [Response], including four fact witness declarations and an expert declaration" and "repeatedly attempts to incorporate by reference arguments and explanation from these declarations." Pet. Reply 26. According to Petitioner, "Qualcomm's swear-behind argument consists almost entirely of conclusory statements alleging that particular claim limitations are shown in Ex. 2006, followed by citations to more detailed explanations in the expert and fact witness declarations." *Id*. at 26–27. Petitioner contends that "[t]his is a clear attempt by Qualcomm to circumvent the 14,000 word limit" and that "[t]he Board should thus consider only the arguments presented in the [Response], and should refuse to consider the arguments incorporated by reference from the various declarations." *Id*. at 27–28.

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[6] *See* Ex. 1001, 2:10–18 ("The layout of the local interconnects for the blocking transistors has proven to be awkward and decreases density. Accordingly, there is a need in the art for improved local interconnect layouts.").

This is not persuasive. As Patent Owner observes, if Petitioner believed Patent Owner had circumvented the word count limit, "it was obligated to raise the issue with Patent Owner such that Patent Owner could 'take reasonable steps to remedy any such issues before approaching the Board' and then 'raise the issue with the Board promptly after discovering the issue.'" PO Sur-Reply 21 (citing Trial Practice Guide Update (August 2018) § II.A.3). We find that, having failed to follow our guidance, Petitioner has waived this complaint.

Moreover, having reviewed the exhibits, including the declarations, we do not agree that Patent Owner has improperly circumvented the word count limit, because the material in the exhibits is the factual support for the swear behind argument, not argument itself, and the amount of factual support is appropriate in the particular circumstances of this case, given the extent and degree of proof required to antedate, and that Patent Owner bears the burden of proof. *See Apator Miitors*, 887 F. 3d at 1297.

5. Conclusion Regarding Antedating

Because we conclude the Patent Owner has established a date of invention that removes Rashed and Lu as prior art, and all grounds require Rashed, we find that Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 4, 8, 12, 13, 15–18, and 20 were unpatentable.

D. Patentability of Claims 3, 9, 10, 14, and 19

Petitioner argues that dependent claims 3, 9, 14, and 19 were anticipated by Rashed, and that claim 10 was obvious in view of Rashed and Nauta.[7] *See* Pet. 37–38, 44–46, 49–51, 56–57, 67–74.

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged or combined in the same way as in the claim, "the reference need not satisfy an *ipsissimis verbis* test," i.e., the terminology used need not be identical. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (citing *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990)). The dispositive question thus is whether one of ordinary skill in the art would reasonably have understood or inferred from a prior art reference that every claim element is disclosed in that reference. *Eli Lilly v. Los Angeles Biomedical Research Inst. at Harbor-UCLA Med. Ctr.*, 849 F.3d 1073, 1074–75 (Fed. Cir. 2017).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter

[7] The Petition also argued that "[t]o the extent that the Patent Owner challenges the anticipation . . . by Rashed because, for instance, Patent Owner considers Rashed's first metal layer M1 not to be the lower-most metal layer . . . , it would have been obvious to APOSITA that Rashed teaches or suggests a first metal layer M1 that is the lower-most metal layer." Pet. 57. Because Patent Owner does not argue that Rashed's first metal layer M1 is not the lower-most metal layer, we need not address obviousness in view of Rashed alone.

pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence.[8] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. The Independent Claims

Because claims 3, 9, and 10 depend, ultimately, from claim 1, and claim 14 depends ultimately from claim 12, we first discuss independent claim 1 and independent claim 12, which the parties argue together, in the context of claim 1. We discuss claim 17, which is in means-plus-function format, separately in the discussion of its dependent claim 19.

a. "[a] circuit comprising"

Petitioner argues that "[t]o the extent . . . the preamble of claim 1 may be limiting, Rashed discloses 'a circuit.'" Pet. 19 (citing Ex. 1003 ¶ 52). We agree that Rashed discloses "a circuit," and Patent Owner does not argue otherwise.

[8] Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.

b. *"a first gate layer arranged according to a gate layer pitch between a second gate layer and a third gate layer"; "a first gate-directed local interconnect arranged between the first gate layer and the second gate layer"; and "a second gate-directed local interconnect arranged between the first gate layer and the third gate layer"*

Regarding the gate layers and gate directed local interconnects, Petitioner cites, for example, the structure depicted in Rashed's Figure 4A, which we annotate with colors below left, next to Figure 4A of the '418 patent, with corresponding structures annotated with like colors:

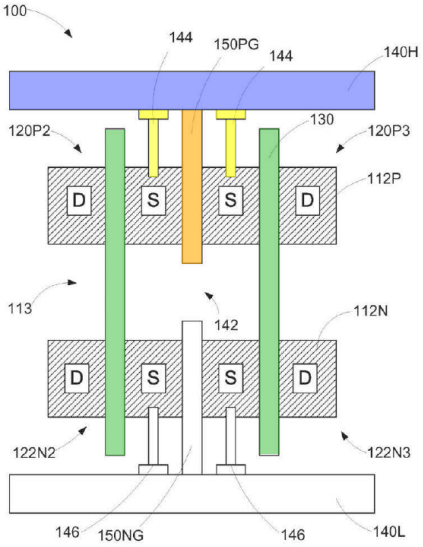

Figure 4A

Figure 4A of Rashed is a schematic depiction of an exemplary semiconductor device. See Ex. 1001, 3:29–31.

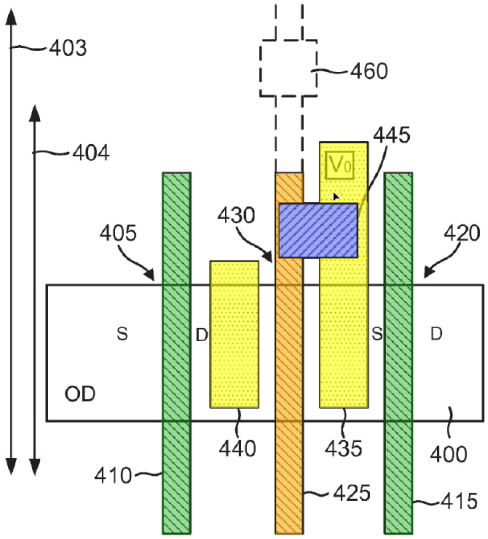

FIG. 4A

Figure 4A of the '418 patent shows "the layout for a pair of transistors in a continuous diffusion region including a blocking transistor." Ex. 1001, 3:9–10.

Petitioner asserts that in Rashed the first "gate layer" would be the structure in orange, the second and third gate layers would be the structures

in green, and the first and second gate directed interconnects would be the structures in yellow. *See* Pet. 20–27. The first gate layer (in orange) is evenly spaced between the second and third gate layers (in yellow) and, thus, is "arranged according to a gate layer pitch between a second gate layer and a third gate layer." Patent Owner does not dispute that the structures highlighted above correspond to the claimed gate layers and gate directed local interconnects (*see* PO Resp. 49–61), and we conclude that Petitioner has shown that Rashed describes these claim elements.

c. "a diffusion-directed local interconnect layer configured to couple the first gate layer to one of the first and second gate-directed local interconnects"

The purple bar shown in our annotated Figure 4A of Rashed is the structure Petitioner identifies as the "diffusion-directed local interconnect layer" that is "configured to couple the first gate layer to one of the first and second gate-directed local interconnects." *See* Pet. 28–29.

According to the reference, "[t]he isolating electrode[] 150PG"—which is the [orange] first gate layer—is "conductively coupled to the [purple] power rails 140H, 140L, respectively, by any of a variety of different conductive structures that are formed in a layer of insulating material positioned above the substrate." Ex. 1005, 5:44–48. The reference also explains that "the source regions of the PFET devices 120P2-3 are coupled to the [purple] power rail 140H by schematically depicted conductive structures 144"—which are the [yellow] gate directed interconnects." *Id*. at 6:32–34.

Patent Owner argues that "it is not enough for Petitioner to show 'power rail' 140H or 140L . . . can be interpreted as indirectly or incidentally

coupling 'isolating electrode' 150PG or 150NG . . . to conductive structure 190P or 190N" because "the phrase 'configured to' in this element 'requir[es] structure designed to or configured to accomplish the specified objective, not simply that they can be made to serve that purpose.'" PO Resp. 56–57.

This argument is not persuasive because we find that Rashed's power rail *is* configured (or designed) to electrically couple the isolating electrodes to the conductive structures. Patent Owner's argument that "[t]he power rail of Rashed is physically constructed for the purpose of providing a source of power (e.g., Vdd or ground) to various components" (PO Resp. 57) is unavailing because, as constructed to provide power to both structures, the power rail *also* electrically couples them. *See* Tr. 10–11 (Patent Owner: "I don't dispute that they're all at the same potential."). It does not matter that "Rashed never states or suggests that these power rails are configured to couple those different components to one another" (PO Resp. 50) because the power rails are, in fact, designed to couple the components together.

Patent Owner also argues that the claim language is "not met simply if a first gate layer is coupled to one of the first and second gate-directed local interconnects" because the claim "requires that the structure or structures that couple those two elements be a diffusion-directed local interconnect layer." PO Resp. 58. Patent Owner argues Petitioner "affirmatively states" that "the power rails 140L and 140H are 'conductively coupled' to the isolating electrodes 150PG and 150NG . . . through conductive contacts" 192P and 192N and that "Petitioner does not assert that the 'diffusion-directed local interconnect layer' is the combination of a power rail and conductive contact." *Id*.

We are not persuaded by this argument because it is not commensurate with the scope of claim 1, which does not recite that the coupling is direct or not reliant on other structures. As Patent Owner has not asked for a claim construction that would limit the claims to direct coupling, we interpret this open-ended claim, as we did at institution, to encompass a diffusion-directed local interconnect that couples the electrodes either directly or through other structures.[9] The power rail is "configured to couple" the gate layer and interconnect because it is part of a conductive path between those structures. If it were not present, for example, then the gate layer and interconnect would not be coupled together. Because it is present, they are coupled.

Further, at oral argument, Patent Owner confirmed that it "do[es] not assert a construction of 'coupled' to require direct coupling" (Tr. 17:18) and we see no material difference between an argument that the coupling does not have to be direct and the argument that the prior art does not describe coupling due to the presence of the conductive contacts.

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[9] *Cf. Asetek Holdings, Inc. v. Coolit Sys.*, No: C-12-4498, 2013 U.S. Dist. LEXIS 170488, at *17 (N.D. Cal. 2013) ("the term 'coupled'—in isolation—could support either direct or indirect connections"); *Silicon Image, Inc. v. Genesis Microchip, Inc.*, No. 3:01-c-266, 2002 U.S. Dist. LEXIS 28916, at *88 (E.D. Va. 2002) (observing that the "common usage of the term 'couple' supports both direct and indirect connections"); *Silicon Graphics, Inc. v. Nvidia Corp.*, 58 F.Supp.2d 331, 346 (D. Del. 1999) (noting that "the ordinary and accustomed meaning of the term 'couple,' even when used in an electronics context does not solely mean 'directly coupled'").

We thus agree with Petitioner that Rashed discloses a diffusion-directed local interconnect layer configured to couple the first gate layer to one of the first and second gate-directed local interconnects.

> *d. "wherein the first gate-directed local interconnect, the second gate-directed local interconnect, and the diffusion-directed local interconnect are all located between a lower-most metal layer and a semiconductor substrate for the circuit"*

For this limitation, Petitioner points to cross-sectional Figures 5A–A, 6A, and 6B, contending that the interconnects are located between a lower-most metal layer ("metal 1 layer 179") and a substrate (113, 112P, or 112N). *See* Pet. 30–33. Patent Owner does not dispute that the structures identified by Petitioner as the interconnects lie between a lowest metal layer and a substrate. We conclude that Petitioner has shown that Rashed describes this arrangement.

2. Claim 3

Claim 3, which depends from claim 1, recites that "the diffusion-directed local interconnect layer is positioned outside of a footprint for the continuous diffusion region."

Petitioner argues that "power rails 140H, 140L are diffusion-directed interconnects" and that "as depicted in [Figures 4A, 4B, and 5A], power rails 140H, 140L are positioned outside the footprint of regions 112P and 112N." Pet. 37.

Patent Owner does not offer arguments specific to claim 3 (*see* PO Resp. 49–77), and we agree with Petitioner that the power rails in Rashed are outside the footprint of the continuous diffusion region.

3. Claim 9

Claim 8 recites that "the first gate layer is the gate layer for a diode-connected transistor." Claim 9, which depends from claim 8, recites "a continuous diffusion region including drain/source terminals for the diode-connected transistor, and wherein the diffusion-directed local interconnect is located outside of a footprint for the continuous diffusion region."

Petitioner argues for claim 8 that "[a]t least because [Rashed's] isolating electrode 150PG is a gate layer for a diodeconnected transistor and isolating electrode 150NG is a gate layer for another diode-connected transistor, Rashed discloses 'the first gate layer is the gate layer for a diode-connected transistor.'" Pet. 44 (citing Ex. 1003 (Liu Decl.) ¶ 86). For claim 9, Petitioner argues that "Rashed discloses 'a continuous diffusion region including drain/source terminals for the diode-connected transistor'" because "active region 112P includes drain/source terminals for a diode-connected transistor, and active region 112N includes drain/source terminals for another diode-connected transistor." *Id*. at 45 (citing Ex. 1003 (Liu Decl.) ¶ 86).

Patent Owner does not offer arguments specific to claim 9 (*see* PO Resp. 49–77), and we agree with Petitioner that Rashed discloses the features of claim 9.

4. Claim 10

Claim 10, which depends from claim 1, recites that "the first gate layer is a gate layer for a first inverter, and wherein the one of the first and second gate-directed local interconnects is a gate-directed local interconnect for an output node for a second inverter."

Petitioner argues that "the common-mode voltage inverter in Nauta has the gates and drains of the respective PFET and NFET of the inverter tied to each other" and that one of skill in the art would have been motivated to add such an arrangement to Rashed for "various reasons" described in Nauta. *See* Pet. 68–73.

Patent Owner does not offer arguments specific to claim 10 (*see* PO Resp. 49–77), and we agree with Petitioner that the combination includes the features of claim 10 and that one of skill in the art would have been motivated to make the combination. *See* Ex. 1003 (Liu Decl.) ¶¶ 96–101.

5. Claim 14

Claim 13 depends from independent claim 12 and recites that "forming the first gate layer forms a gate for a blocking transistor." Claim 14 depends from claim 13 and adds "forming a continuous diffusion region," where "forming the first gate layer forms a gate for a transistor having a pair of drain/source terminals in the continuous diffusion region" and "forming the diffusion-directed local interconnect comprises forming [it] outside of a footprint for the continuous diffusion region."

For claim 13, Petitioner refers to its arguments for claim 1. *See* Pet. 49. For claim 14, Petitioner argues that Rashed's "isolating electrode 150PG is a gate layer for a blocking transistor formed respectively in diffusion region 112P" and refers to its analysis of claim 3 for the recitation "forming the diffusion-directed local interconnect outside of a footprint for the continuous diffusion region." *See* Pet. 50–51.

Patent Owner does not offer arguments specific to claim 14, but does argue with respect to claim 12 that "forming . . . to" requires "structure designed to or configured to accomplish the specified objective, not simply

that they can be made to serve that purpose." PO Resp. 59. Patent Owner also argues that claim 12 "requires that the structure or structures that couple the first gate layer to one of the first and second gate-directed local interconnects be [a] diffusion-directed local interconnect layer." Prelim. Resp. 60.

Patent Owner's arguments mirror those made in connection with claim 1, and we find them unpersuasive for the same reasons articulated in Section II.D.1.c.

6. Claim 19

Independent claim 17 is similar to claims 1 and 12, but is written in means plus function format. Patent Owner argues that "the corresponding structures of [the "means for coupling"] element . . . are the diffusion-directed local interconnects described in the '418 Patent" and that "[n]one of [those] the diffusion-directed local interconnects . . . rely upon other structures, for example, an intermediate connection such as a 'via' (or contact hole), to couple to either a gate-directed local interconnect or gate layer." PO Resp. 60–61. Petitioner's Reply does not address this issue.

We agree with Patent Owner that Petitioner has not shown how Rashed describes the claimed "means-for-coupling." As Patent Owner argues, none of the identified structures in the '418 patent rely on additional structures for the coupling, and Petitioner has not argued that Rashed's arrangement, which does rely on an intermediate structure, would be an equivalent to the disclosed structures.

We accordingly conclude that Petitioner has not shown that claim 17 is anticipated by Rashed and, because claim 17 has not been shown to be

anticipated, claim 19, which depends from and includes all of the limitations of claim 17, has not been shown to be anticipated either.

7. Conclusion on the Patentability of Claims 3, 9, 10, 14, and 19

For the reasons above, we conclude that Petitioner has shown by a preponderance of the evidence that claims 3, 9, 10, and 14 of the '418 patent are unpatentable. Petitioner has not shown that claim 19 of the '418 patent is unpatentable.

E. Motions to Seal

At the time it filed its Response, Patent Owner moved to seal "Exhibits 2005–2007, 2009, 2010, 2011A–2011C, 2012, 2014A–2014C, 2015, 2016A, 2016C, 2017–2021, 2022A, 2022B, 2023–2026, 2027A, 2027B, 2028A, 2028B, 2029–2032, 2034–2041, 2043–2052, 2053A–2053C, 2054, 2055, 2056A, 2056B, 2057, 2058, and 2060–2063." Paper 19 ("PO Mot. to Seal") 1. At the time it filed its Reply, Petitioner filed a motion to "seal its Petitioner Reply and supporting Exhibits APPLE-1015 through 1019." Paper 34 ("Pet. Mot. to Seal") 1. Neither motion is opposed.

All papers are available for public access by default. *See* 35 U.S.C. § 316(a)(1). A party may file a motion to seal concurrent with the filing of the confidential information at issue, and the information is sealed pending the motion's outcome. 37 C.F.R. § 42.54. Commercial information may be confidential information. *See* 37 C.F.R. § 42.54(7).

The standard for granting a motion to seal is "good cause." 37 C.F.R. § 42.54(a). For instance, we consider whether the movant has adequately shown that "(1) the information sought to be sealed is truly confidential, (2) a concrete harm would result upon public disclosure, (3) there exists a

genuine need to rely in the trial on the specific information sought to be sealed, and (4) on balance, an interest in maintaining confidentiality outweighs the strong public interest in having an open record." *Argentum Pharms. LLC v. Alcon Research, Ltd.*, IPR2017-01053, Paper 27 at 4 (PTAB Jan. 19, 2018) (informative).

Patent Owner argues there is good cause for sealing the exhibits because "Patent Owner is swearing behind certain prior art relied upon in the Petition" and the exhibits to support that argument "consist of and are permeated with commercially-sensitive information that is still used in it[s] products today, and for certain of which Patent Owner owes a duty of confidentiality to third party Taiwan Semiconductor Manufacturing Company ('TSMC')." *See* PO Mot. to Seal 3–6. Patent Owner also argues that "[t]he public's interest in maintaining a complete and understandable record in this proceeding is not harmed by maintaining the Confidential Documents under seal" because "Patent Owner's Response and Dr. Lall's declaration, each of which are public, provide summaries of relied-upon portions of the Confidential Documents" and the Board's "reliance on the Confidential Documents does not necessitate the full disclosure to the public of the Confidential Documents." *Id*. at 7.

Petitioner states that it is "not in a position to make the necessary representations about why [its filings] may warrant sealing," but that "because [they discuss] material filed by Patent Owner under seal, Petitioner has filed its Petitioner Reply and the supporting evidence under seal." Pet. Mot. to Seal 2.

Based on the parties' representations, we conclude that the papers proposed to be sealed include commercially-sensitive information that is not

publicly available, that the information sought to be sealed reflects confidential business information of Patent Owner and/or TSMC, and that "an interest in maintaining confidentiality outweighs the strong public interest in having an open record" here. *See Argentum*, Paper 27 at 4. We thus determine that good cause exists for sealing and grant the Motions to Seal.

Patent Owner also submits, as Appendix A to its motion, "[a] copy of the Board's Default Protective Order, as modified by agreement among Patent Owner and Petitioner." PO Mot. to Seal 2. The proposed modifications add an attorney's eyes only tier and provisions that govern the exchange of documents and information among the parties. *See* PO Mot. to Seal, Appendix B.

Patent Owner asserts that "[g]ood cause exists for the modifications because the Confidential Documents consist of and are permeated with confidential and highly-sensitive business and technical information of Patent Owner and third-party Taiwan Semiconductor Manufacturing Company ('TSMC') that, if shared with Petitioner's in-house counsel and business personnel, would harm TSMC's and Patent Owner's respective businesses" and "because the circuit layout (GDS) Patent Owner relies upon is too large to upload to E2E and too sensitive to transmit electronically, necessitating special procedures to make it available for inspection by Petitioner." PO Mot. to Seal 2–3.

We conclude that the modifications to the default order are appropriate under the circumstances and thus enter the proposed protective order attached as Appendix A to Patent Owner's motion. Nothing in that order shall, however, impose any obligation on the Board or any Office

employee that does not already exist under our rules and the default protective order.

The parties are reminded that **confidential information subject to a protective order ordinarily becomes public 45 days after a final judgment in a trial**. *See* Patent Trial and Appeal Board Consolidated Trial Practice Guide (November 2019) 19–22.[10] To avoid that, a party may file a motion to expunge confidential information from the record before the information becomes public. *See* 37 C.F.R. § 42.56.

[10] Available at <https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance>.

III. CONCLUSION

Claims 1, 2, 4, 5, 8, 12, 13, 15–19, and 20 have not been shown to be unpatentable. Claims 3, 9, 10, and 14 have been shown to be unpatentable. The results are summarized below.

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3, 5, 8, 9, 12–14, 16–19	102	Rashed	3, 9, 14	1, 2, 4, 5, 8, 12, 13, 15–19, 20
1–3, 5, 8, 9, 12–14, 16–19	103	Rashed	N/A	N/A
4, 15, 20	103	Rashed, Lu		4, 15, 20
10	103	Rashed, Nauta	10	
Overall Outcome			3, 9, 10, 14	1, 2, 4, 5, 8, 12, 13, 15–19, 20

IV. ORDER

For the reasons given, it is:

ORDERED that claims 3, 9, 10, and 14 of U.S. Patent 9,024,418 B2 are unpatentable;

ORDERED that claims 1, 2, 4, 5, 8, 12, 13, 15–19, and 20 of U.S. Patent 9,024,418 B2 have not been shown to be unpatentable;

ORDERED that Patent Owner's Motion to Seal and Petitioner's Motion to Seal are *granted* and the Protective Order attached as Appendix A to Paper 19 is *entered*; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.[11]

[11] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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